WTQD400-LR4

QSFP-DD 400Gb/s LR4 10km Transceiver / PRODUCT FEATURES

Part Number
WTQD400-LR4



1. Product Overview

Features

- 400G-LR4 compliant
- 4x 53.125 GBd PAM4
- 400GAUI-8 compliant
- 8x 26.5625 GBd PAM4
- QSFP-DD MSA compliant
- LC connector
- Power consumption <12 W
- Operating case temperature 0 to 70 ºC
- CMIS 4.0 management interface

Applications

- High performance computing interconnect
- Data Centers
- Cloud Networks

2. Ordering Information

Part No.	Description
WTQD400-LR4	400G-LR4 QSFP-DD 10km Single Mode Fiber Transceiver, 0 to 70 ºC

3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	Vcc	0	+3.6	V	
Storage Temperature		-40	85	°C	
Optical Receiver Input		-	+6.1	dBm	Average, each lane

4. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNRmod	-	-	66	mV	10 Hz –10 MHz
Power Consumption	P_6	-	-	12	W	
Instantaneous peak current	Icc_ip_6			4800	mA	
Sustained peak current	Icc-sp_6			3960	mA	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply Current	Icc-6	--	-	3827.8	mA	Steady state
Case Temperature	TC	0	25	70	°C	

5. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Channel data rate	fDC	106.25	106.25	106.25	Gbit/s	
Signaling rate, each lane	fSG	53.125	53.125	53.125	GBd	PAM4
Signal speed variation from nominal, each lane	⊿fSG	-100		+100	ppm	
Lane 0	□CT0	1264.5		1277.5	nm	
Lane 1	□CT1	1284.5		1297.5	nm	
Lane 2	□CT2	1304.5		1317.5	nm	
Lane 3	□CT3	1324.5		1337.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Total average launch power				11.1	dBm	
Average launch power, each lane		-2.7		5.1	dBm	Note 1
Outer Optical Modulation Amplitude (OMAouter), each lane		0.3		4.4	dBm	for TDECQ <1.4 dB
Outer Optical Modulation Amplitude (OMAouter), each lane		-1.1 + TDECQ		4.4	dBm	for 1.4 dB ≤ TDECQ ≤ 3.9 dB
Difference in launch power between any two lanes (OMAouter)				4	dB	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.9	dB	
Transmitter eye closure for PAM4, each lane	TECQ			3.9	dB	
| TDECQ – TECQ |				2.5	dB	
Average optical output power of OFF Transmitter, each lane	Poff			-16	dBm	
Extinction Ratio, each lane	ER	3.5			dB	
Transmitter transition time				17	ps	
Transmitter over/under-shoot				25	%	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Transmitter peak-to-peak power				5.2	dBm	
RIN15.6OMA				-136	dB/Hz	
Optical return loss tolerance				15.6	dB	
Transmitter reflectance				-26	dB	Note 2
Average receive power, each lane		–9		5.1	dBm	Note 3
Receive power (OMAouter) , each lane				4.4	dBm	
Difference in receive power between any two lanes (OMAouter)				4.3	dB	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane		Max -6.8	Max -6.8	Max -6.8	dBm	for TECQ <1.4 dB, Note 4
Receiver sensitivity (OMAouter), each lane		Max (-8.2 + TECQ)	Max (-8.2 + TECQ)	Max (-8.2 + TECQ)	dBm	for 1.4 dB ≤ TECQ ≤ 3.9 dB, Note 4
Stressed receiver sensitivity, each lane (OMAouter)				-4.3	dBm	Note 4, 5
Conditions of stressed receiver sensitivity test (note 6)	Conditions of stressed receiver sensitivity test (note 6)	Conditions of stressed receiver sensitivity test (note 6)	Conditions of stressed receiver sensitivity test (note 6)	Conditions of stressed receiver sensitivity test (note 6)	Conditions of stressed receiver sensitivity test (note 6)	Conditions of stressed receiver sensitivity test (note 6)
Stressed eye closure for PAM4, lane under test	SECQ	3.9	3.9	3.9	dB	
OMAouter of each aggressor lane		-0.4	-0.4	-0.4	dBm	

6. Pin Descriptions

Version No.	Date	Description
1.0	May 17, 2023	Specification datasheet

7. Additional Specifications

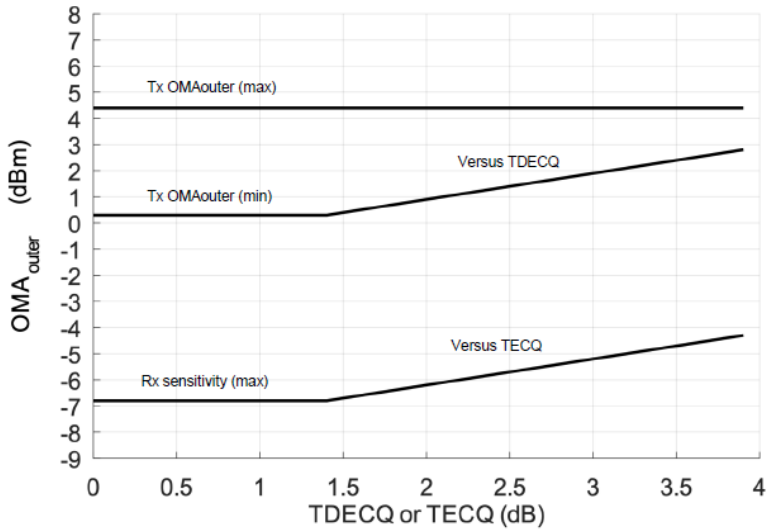
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Receiver Loss of Signal Indicator Assert Level	RX_LOS	-30	-	-10.3	dBm	Average power
Receiver Loss of Signal Indicator De-assert Level	RX_LOS	-	-	-9.8	dBm	Average power
Hysteresis	RX_LOS	0.5	-	-	dB	

8. Additional Specifications

Parameter	Min.	Typ.	Max.	Unit	Remarks
Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]
Signaling rate per lane (range)	-100ppm	26.5625	+100ppn	GBd	
AC Common-mode output voltage (RMS)	-	-	17.5	mV	
Differential peak-to-peak output voltage	-	-	900	mV	
Near-end ESMW (Eye symmetry mask width)	0.265	-	-	UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)	0.2	-	-	UI	
Far-end Eye height, differential	30	-	-	mV	
Far-end pre-cursor ISI ratio	-4.5	-	2.5	%	
Differential output return loss	Equation (83E-2)	-	-	dB	Note 2
Common to differential mode conversion return loss	Equation (83E-3)	-	-	dB	Note 2
Differential termination mismatch	-	-	10	%	
Transition time (20% to 80%)	9.5	-	-	ps	
DC common mode voltage	-350	-	2850	mV	
Module input (each lane)	Module input (each lane)	Module input (each lane)	Module input (each lane)	Module input (each lane)	Module input (each lane)
Signaling rate per lane (range)	-100ppm	26.5625	+100ppm	GBd	
Differential pk-pk input voltage tolerance	900	-	-	mV	at TP1a
Differential input return loss	Equation (83E-5)	-	-	dB	at TP1, Note 2
Differential to common mode input return loss	Equation (83E-6)	-	-	dB	at TP1, Note 2
Differential termination mismatch	-	-	10	%	at TP1
ESMW (Eye symmetry mask width)	0.22	-	-	UI	at TP1a
Eye width	0.22	-	-	UI	at TP1a
Applied pk-pk sinusoidal jitter	Table 120E–6	Table 120E–6	Table 120E–6	MHz, UI	at TP1a
Eye height	32	-	-	mV	at TP1a
Single-ended input voltage tolerance range	-0.4	-	3.3	V	at TP1a

Parameter	Min.	Typ.	Max.	Unit	Remarks
DC common mode voltage	-350	-	2850	mV	at TP1

9. Optical Power Limits versus TDECQ or TECQ



10. Pin Descriptions

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

11. Pin Diagram

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69	LVTTL-I	ePPS	Precision Time Protocol (PTP) reference clock input	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

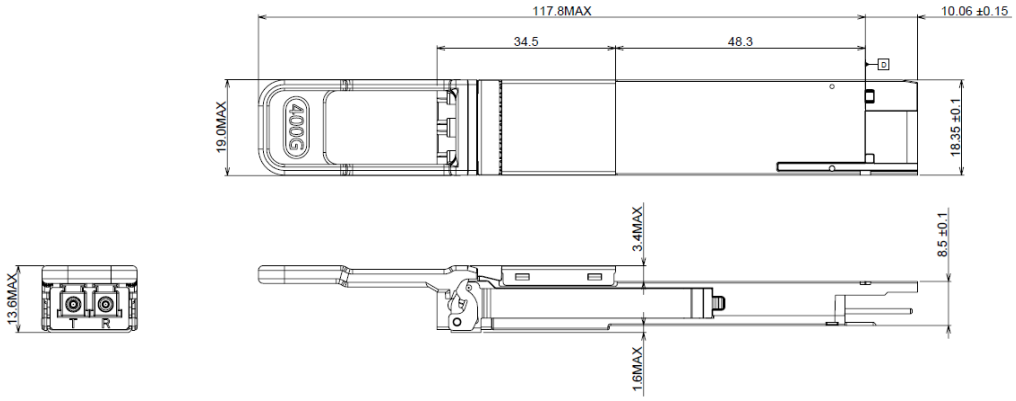
Note 1: QSFP-DD uses common ground (GND)for all signals and supply (power). All are common within the QSFP-DD module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 shall be applied concurrently. Requirements defined for the host side of the Host Card Edge Connector are listed in Table 7. VccRx, VccRx1, Vcc1, Vcc2, VccTx and VccTx1 may be internally connected within the module in any combination. The connector Vcc pins are each rated for a maximum current of 1000 mA.

Note 3: All Vendor Specific, Reserved, No Connect and ePPS (if not used) pins may be terminated with 50 Ohms to ground on the host. Pad 65 (No Connect) shall be left unconnected within the module. Vendor specific and Reserved pads shall have an impedance to GND that is greater than 10 kOhms and less than 100 pF.

Note 4: Plug Sequence specifies the mating sequence of the host connector and module. The sequence is 1A, 2A, 3A, 1B, 2B, 3B. (see Figure 2 for pad locations) Contact sequence A will make, then break contact with additional QSFP-DD pads. Sequence 1A,1B will then occur simultaneously, followed by 2A,2B,followed by 3A,3B.

12. Mechanical Specifications



13. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek