400Gb/s QSFP-DD FR4 2km SMF Optical Transceiver WT-DQ4CNT-N00



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1. Product Overview

General Description

This product is a 400Gb/s Quad Small Form Factor Pluggable-double density (QSFP-DD) optical module designed for 2km optical communication applications. The module converts 8 channels of 50Gb/s (PAM4) electrical input data to 4 channels of CWDM optical signals, and multiplexes them into a single channel for 400Gb/s optical transmission. Reversely, on the receiver side, the module optically de-multiplexes a 400Gb/s optical input into 4 channels of CWDM optical signals, and converts them to 8 channels of 50Gb/s (PAM4) electrical output data.

The central wavelengths of the 4 CWDM channels are 1271, 1291, 1311 and 1331 nm as members of the CWDM wavelength grid defined in ITU-T G.694.2. It contains a duplex LC connector for the optical interface and a 76-pin connector for the electrical interface. To minimize the optical dispersion in the long-haul system, single-mode fiber (SMF) has to be applied in this module. Host FEC is required to support up to 2km fiber transmission

The product is designed with form factor, optical/electrical connection and digital diagnostic interface according to the QSFP-DD Multi-Source Agreement (MSA) Type 2. It has been designed to meet the harshest external operating conditions including temperature, humidity and EMI interference.

Functional Description

Features

- QSFP-DD MSA compliant
- 4 CWDM lanes MUX/DEMUX design
- 100G Lambda MSA 400G-FR4 Specification compliant
- Up to 2km transmission on single mode fiber (SMF) with FEC
- Operating case temperature: 0 to 70oC
- 8x53.125Gb/s electrical interface (400GAUI-8)
- Data Rate 106.25Gbps (PAM4) per channel.
- Maximum power consumption 12W
- Duplex LC connector
- RoHS compliant

Applications

- Data Center Interconnect
- 400G Ethernet
- InfiniBand interconnects
- Enterprise Networking

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units	Notes
Storage Temperature	TS	-40	85	degC	
Operating Case Temperature	TOP	0	70	degC	
Power Supply Voltage	VCC	-0.5	3.6	V	
Relative Humidity (non-condensation)	RH	0	85	%	

Parameter	Symbol	Min	Max	Units	Notes
Damage Threshold, each Lane	THd	4.5		dBm	

3. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Operating Case Temperature	TOP	0		70	degC	
Power Supply Voltage	VCC	3.135	3.3	3.465	V	
Data Rate, each Lane			26.5625		GBd	PAM4
Data Rate Accuracy		-100		100	ppm	
Pre-FEC Bit Error Ratio				2.4x10-4		
Post-FEC Bit Error Ratio				1x10-12		1
Link Distance	D	0.002		2	km	2

4. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Units	Notes
Wavelength Assignment	L0	1264.5	1271	1277.5	nm	
Wavelength Assignment	L1	1284.5	1291	1297.5	nm	
Wavelength Assignment	L2	1304.5	1311	1317.5	nm	
Wavelength Assignment	L3	1324.5	1331	1337.5	nm	
Transmitter	Transmitter	Transmitter	Transmitter	Transmitter	Transmitter	Transmitter
Data Rate, each Lane		53.125 ± 100 ppm	53.125 ± 100 ppm	53.125 ± 100 ppm	GBd	
Modulation Format		PAM4	PAM4	PAM4		
Side-mode Suppression Ratio	SMSR	30			dB	
Total Average Launch Power	PT			9.3	dBm	
Average Launch Power, each Lane	PAVG	-3.3		3.5	dBm	1
Outer Optical Modulation Amplitude (OMAouter), each Lane	POMA	-0.3		3.7	dBm	2
Launch Power in OMAouter minus TDECQ, each Lane for ER ≥ 4.5dB for ER < 4.5dB		-1.7 -1.6			dBm	

Parameter	Symbol	Min	Typical	Max	Units	Notes
Transmitter and Dispersion Eye Closure for PAM4, each Lane	TDECQ			3.4	dB	
TDECQ – 10*log10(Ceq), each Lane				3.4	dB	3
Extinction Ratio	ER	3.5			dB	
Difference in Launch Power between any Two Lanes (OMAouter)				4	dB	
RIN17.1OMA	RIN			-136	dB/Hz	
Optical Return Loss Tolerance	TOL			17.1	dB	
Transmitter Reflectance	RT			-26	dB	
Transmitter Transition Time				17	ps	
Average Launch Power of OFF Transmitter, each Lane	Poff			-20	dBm	
Receiver	Receiver	Receiver	Receiver	Receiver	Receiver	Receiver
Data Rate, each Lane		53.125 ± 100 ppm	53.125 ± 100 ppm	53.125 ± 100 ppm	GBd	

5. Recommended Operating Conditions

Modulation Format		PAM4	PAM4	PAM4		
Damage Threshold, each Lane	THd	4.5			dBm	4
Average Receive Power, each Lane		-7.3		3.5	dBm	5
Receive Power (OMAouter), each Lane				3.7	dBm	
Difference in Receiver Power between any Two Lanes (OMAouter)				4.1	dB	
Receiver Sensitivity (OMAouter), each Lane	SEN			Equation (1)	dBm	6
Stressed Receiver Sensitivity (OMAouter), each Lane	SRS			-2.6	dBm	7
Receiver Reflectance	RR			-26	dB	
LOS Assert	LOSA	-20			dBm	
LOS De-assert	LOSD			-10.3	dBm	
LOS Hysteresis	LOSH	0.5			dB	

Modulation Format		PAM4	PAM4	PAM4		
Stressed Conditions for Stress Receiver Sensitivity (Note 8)	Stressed Conditions for Stress Receiver Sensitivity (Note 8)	Stressed Conditions for Stress Receiver Sensitivity (Note 8)	Stressed Conditions for Stress Receiver Sensitivity (Note 8)	Stressed Conditions for Stress Receiver Sensitivity (Note 8)	Stressed Conditions for Stress Receiver Sensitivity (Note 8)	Stressed Conditions for Stress Receiver Sensitivity (Note 8)
Stressed Eye Closure for PAM4 (SECQ), Lane under Test			3.4		dB	
SECQ – 10*log10(Ceq), Lane under Test				3.4	dB	
OMAouter of each Aggressor Lane			1.5		dBm	

6. Recommended Operating Conditions

Parameter	Test Point	Min	Typical	Max	Units	Notes
Power Consumption				12	W	
Supply Current	Icc			3.64	A	
Transmitter (each Lane)	Transmitter (each Lane)	Transmitter (each Lane)	Transmitter (each Lane)	Transmitter (each Lane)	Transmitter (each Lane)	Transmitter (each Lane)
Signaling Rate, each Lane	TP1	26.5625 ± 100 ppm	26.5625 ± 100 ppm	26.5625 ± 100 ppm	GBd	
Differential pk-pk Input Voltage Tolerance	TP1a	900			mVpp	1
Differential Termination Mismatch	TP1			10	%	
Differential Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-5)			dB	
Differential to Common Mode Input Return Loss	TP1	IEEE 802.3-2015 Equation (83E-6)			dB	
Module Stressed Input Test	TP1a	See IEEE 802.3bs 120E.3.4.1	See IEEE 802.3bs 120E.3.4.1	See IEEE 802.3bs 120E.3.4.1		2
Single-ended Voltage Tolerance Range (Min)	TP1a	-0.4 to 3.3	-0.4 to 3.3	-0.4 to 3.3	V	
DC Common Mode Input Voltage	TP1	-350		2850	mV	3
Receiver (each Lane)	Receiver (each Lane)	Receiver (each Lane)	Receiver (each Lane)	Receiver (each Lane)	Receiver (each Lane)	Receiver (each Lane)
Signaling Rate, each lane	TP4	26.5625 ± 100 ppm	26.5625 ± 100 ppm	26.5625 ± 100 ppm	GBd	
Differential Peak-to-Peak	TP4			900	mVpp	
AC Common Mode Output Voltage, RMS	TP4			17.5	mV	
Differential Termination Mismatch	TP4			10	%	
Differential Output Return Loss	TP4	IEEE 802.3- 2015 Equation (83E-2)				

Parameter	Test Point	Min	Typical	Max	Units	Notes
Common to Differential Mode Conversion Return Loss	TP4	IEEE 802.3- 2015 Equation (83E-3)				
Transition Time, 20% to 80%	TP4	9.5			ps	
Near-end Eye Symmetry Mask Width (ESMW)	TP4		0.265		UI	
Near-end Eye Height, Differential	TP4	70			mV	
Far-end Eye Symmetry Mask Width (ESMW)	TP4		0.2		UI	
Far-end Eye Height, Differential	TP4	30			mV	
Far-end Pre-cursor ISI Ratio	TP4	-4.5		2.5	%	
Common Mode Output Voltage (Vcm)	TP4	-350		2850	mV	3

7. Recommended Operating Conditions

Parameter	Symbol	Min	Max	Units	Notes
Temperature monitors absolute error	DMI_Temp	-3	3	degC	Over operating temperature range
Supply voltage monitor absolute error	DMI _VCC	-0.1	0.1	V	Over full operating range
Channel RX power monitor absolute error	DMI_RX_Ch	-2	2	dB	1
Channel Bias current monitor	DMI_Ibias_Ch	-10%	10%	mA	
Channel TX power monitor absolute error	DMI_TX_Ch	-2	2	dB	1

8. Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	

Pin	Logic	Symbol	Description	Plug Sequence	Notes
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16	GND	Ground	1B		1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	

Pin	Logic	Symbol	Description	Plug Sequence	Notes
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	1
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3

Pin	Logic	Symbol	Description	Plug Sequence	Notes
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For Future Use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

9. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek