WincoTek High TX Power 400G ZR and OpenZR+

QSFP-DD DCO Product

Part Number WT-QDD400ZRCH1



1. Product Overview

This document describes the product specifications for 400G ZR and OpenZR+ QSFP-DD DCO modules based on DP-16QAM supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. Chromatic dispersion compensation can be applied to the receive side of the demodulator. This module is managed utilizing the Two Wire Interface that is specified in the Common Management Interface Specification (CMIS).

The module uses a 76-pin QSFP-DD MSA QSFP-DD Hardware Specification connector for all electrical interfaces with the host card, whereas the optical interfaces on the line side are provided through the optical receptacles on the QSFP-DD. The module can be portioned into three functional parts: TX path, RX path and Control & Power block.

Module Descriptions

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Path Descriptions

Features

- Support Flex-grid channel spacing DWDM in C-band
- Support Client-side Interfaces: 1*400GAUI-8 for 400G ZR, 1*400GAUI-8/4*100GAUI-2 for 400G OpenZR+
- Support Line-side: DP-16QAM with CFEC(ZR), DP-16QAM with Ofec (OpenZR+)
- High TX Power up to +3dBm
- Integrated TOF is optional
- 76pin QSFP-DD MSA compliant connector
- Compliant to CMIS 5.0
- Compliant to OIF Implementation Agreement for Coherent CMIS, Rev 01.1 9.
- OIF-400ZR-02.0
- OIF OpenZRplus_2p0
- RoHS compliant

Applications

- The application field of the module is widely used from short haul (ZR) to Metro (MR) interconnects. As shown in figure1, it is comprised of high-data lanes, a single 3.3V power supply, an IIC interface for module control and status report, and dedicated alarm and control pins (not shown on the figure1).
- Figure1: Functional Diagram of Module

2. Ordering Information

Part Number	Description
WT-QDD400ZRCH1	Single rate 400Gb/s, coherent high TX power QSFP-DD ZR with CFEC, 0~70C
WT-QDD400ZRCH2	Single rate 400Gb/s, coherent high TX power QSFP-DD ZR integrated TOF with CFEC, 0~70C

Part Number	Description
WT-QDD400ZPCH1	Single rate 400Gb/s, coherent high TX power QSFP-DD OpenZR+ with oFEC, 0~70C
WT-QDD400ZPCH2	Single rate 400Gb/s, coherent high TX power QSFP-DD OpenZR+ integrated TOF with oFEC, 0~70C

3. Ordering Information

Host Interface	Application Data Rate	Lane Count	Lane Signaling Rate	Modulation
1*400GAUI-8	425.00 Gb/s	8	26.5625 GBaud(+/- 100 ppm)	PAM4
4*100GAUI-2	4*106.25 Gb/s	8	26.5625 GBaud(+/- 100 ppm)	PAM4

4. Absolute Maximum Ratings

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	℃	
Storage Humidity (Relative)	-	85	%	no-Condensing
Case Temperature	0	75	℃	
Operating Humidity (Relative)	-	85	%	no-Condensing
Short term Operating Case Temperature		80	℃	<24 hours
Power Supply Absolute Range	-0.3	3.63	V	
RX Optical Maximum Input Power	-	10	dBm	

5. Recommended Operating Conditions

Parameter	Min	Max	Unit	Note
Operating Case Temperature	0	70	℃	
Operating Humidity (Relative)	-	85	%	no-Condensing
Power Supply Operating Range	3.135	3.465	V	
RX Optical Input Power	-	0	dBm	

6. Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit	Note
3.3V DC Power Supply Voltage	3.135	3.3	3.465	V	
3.3V DC Power Supply Current			8	A	

Parameter	Min	Typ.	Max	Unit	Note
Power Dissipation@400G ZR		16	18	W	
Power Dissipation@400G OpenZR+		17	21.5	W	
Low Power Consumption			1.5	W	
Module Inrush Current			100	mA/us	
Turn-off Current	-100			mA/us	
Power Supply Noise			25	mV	

7. Recommended Operating Conditions

Parameter	Min	Typ.	Max	Unit	Note
Electrical Characteristics for Transmitter	Electrical Characteristics for Transmitter	Electrical Characteristics for Transmitter	Electrical Characteristics for Transmitter	Electrical Characteristics for Transmitter	Electrical Characteristics for Transmitter
Signal Rate, each Lane	26.5625±100ppm	26.5625±100ppm	26.5625±100ppm	GBaud	
Differential Peak-Peak Input Voltage Tolerance			900	mVpp	
Electrical Characteristics for Receiver	Electrical Characteristics for Receiver	Electrical Characteristics for Receiver	Electrical Characteristics for Receiver	Electrical Characteristics for Receiver	Electrical Characteristics for Receiver
Signal Rate, each Lane	26.5625±100ppm	26.5625±100ppm	26.5625±100ppm	GBaud	
Differential Peak-Peak Input Voltage Tolerance		750	900	mVpp	
Transition Time, 20% to 80%		9.5		ps	

8. Optical Parameters

Parameter	Min	Typ.	Max	Unit	Notes
Transmitter Frequency Range	191.3	193.7	196.1	THz	C band 75GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
Laser Frequency Stability	-1.8		1.8	GHz	Frequency stability relative to ITU grid.
Laser Frequency Accuracy	-1.8		1.8	GHz	
Laser Frequency Fine Tuning Range	-6.0		6.0	GHz	
Fine Tuning Resolution		100		MHz	

Parameter	Min	Typ.	Max	Unit	Notes
Channel Tuning Speed	-		60	s	
Laser LineWidth			100	kHz	
Transmitter Output Power Range	-5		+3	dBm	
Transmitter Output Disable Time			180	ms	
Output Power Stability	-0.5		0.5	dB	Difference over temperature, time, wavelength and aging.
Output Power Accuracy	-2		2	dB	Difference between the set value and actual value over aging.
Transmitter Turn-up Time from Cold Start	-		120	s	
Transmitter OSNR (Inband)	34		-	dB/0.1nm	
Transmitter OSNR (Out-of-band)	Order-specific		-	dB/0.1nm	WT-QDD400ZPCH2 TOF variant; confirmed limits supplied with order
Transmitter Back Reflectance	-		-24	dB	
Transmitter Output Power with TX Disabled	-		-20	dBm	
Transmitter Polarization Dependent Power	-		1.5	dB	Power deference between X and Y polarization

9. 400G ZR Receiver Optical Parameters (CFEC)

Parameter	Min	Typ.	Max	Unit	Notes
Receiver Frequency Range	191.3	193.7	196.1	THz	
Input Power Range	-12		0	dBm	Signal power of the channel at the OSNR Penalty < 0.5dB
OSNR Sensitivity		24	26	dB/0.1nm	
Receiver Sensitivity			-20	dBm	Input power needed to achieve post FEC BER < 1E-15 when OSNR Tolerance >26dB/0.1nm
CD Tolerance	2400			ps/nm	Tolerance to CD with 0.5 dB penalty to OSNR sensitivity when change in SOP is1 rad/ms.
PMD Tolerance	10			ps	Tolerance to PMD with < 0.5 dB penalty to OSNR sensitivity.

Parameter	Min	Typ.	Max	Unit	Notes
Peak PDL Tolerance	3.5			dB	Tolerance to peak PDL with < 1.8 dB penalty to OSNR sensitivity when change in SOP is < =1 rad/ms.
Tolerance to Change in SOP	50		-	rad/ms	
Input Power Transient Tolerance	-2		2	dB	Tolerance to change in input power with < 0.5 dB penalty to OSNR sensitivity.
Input Power Reading Accuracy	-2		2	dB	
Optical Return Loss	20			dB	Optical reflectance at Rx connector input.
Receiver Turn-up Time from Cold Start	-		120	s	From module reset, with valid optical input signal present.

10. 400G OpenZR+ Receiver Optical Parameters (oFEC)

Parameter	Min	Typ.	Max	Unit	Notes
Receiver Frequency Range	191.3	193.7	196.1	THz	
Input Power Range	-12		0	dBm	Signal power of the channel at the OSNR Penalty < 0.5dB
OSNR Sensitivity		22	24	dB/0.1nm	
Receiver Sensitivity			-20	dBm	Input power needed to achieve post FEC BER < 1E-15 when OSNR Tolerance >26dB/0.1nm
CD Tolerance	9000			ps/nm	Tolerance to CD with 0.5 dB penalty to OSNR sensitivity when change in SOP is1 rad/ms.
PMD Tolerance	20			ps	Tolerance to PMD with < 0.5 dB penalty to OSNR sensitivity.
Peak PDL Tolerance	3.5			dB	Tolerance to peak PDL with < 1.8 dB penalty to OSNR sensitivity when change in SOP is < =1 rad/ms.
Tolerance to Change in SOP	50		-	rad/ms	
Input Power Transient Tolerance	-2		2	dB	Tolerance to change in input power with < 0.5 dB penalty to OSNR sensitivity.
Input Power Reading Accuracy	-2		2	dB	
Optical Return Loss	20			dB	Optical reflectance at Rx connector input.

Parameter	Min	Typ.	Max	Unit	Notes
Receiver Turn-up Time from Cold Start	-		120	s	From module reset, with valid optical input signal present.

11. Optical Parameters

Parameter	Min	Max	Unit	Note
Insertion Force		90	N	
Extraction Force		50	N	
Retention Force	90		N	

12. Pin Descriptions

Pin#	Logic	Symbol	Description	Plug Sequence
1		GND	Ground	1B
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B
4		GND	Ground	1B
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B
7		GND	Ground	1B
8	LVTTL-I	ModSelL	Module Select	3B
9	LVTTL-I	ResetL	Module Reset	3B
10		VccRx	+3.3V Power Supply Receiver	2B
11	LVCMOS- I/O	SCL	2-wire serial interface clock	3B
12	LVCMOS- I/O	SDA	2-wire serial interface data	3B
13		GND	Ground	1B
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B
15	CML-O	Rx3n	Receiver Inverted Data Output	3B
16	GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B
18	CML-O	Rx1n	Receiver Inverted Data Output	3B
19		GND	Ground	1B
20		GND	Ground	1B
21	CML-O	Rx2n	Receiver Inverted Data Output	3B

Pin#	Logic	Symbol	Description	Plug Sequence
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B
23		GND	Ground	1B
24	CML-O	Rx4n	Receiver Inverted Data Output	3B
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B
26		GND	Ground	1B
27	LVTTL-O	ModPrsL	Module Present	3B
28	LVTTL-O	IntL	Interrupt	3B
29		VccTx	+3.3V Power supply transmitter	2B
30		Vcc1	+3.3V Power supply	2B
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B
32		GND	Ground	1B
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B

13. Pin Descriptions

34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
35		GND	Ground	1B
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B
38		GND	Ground	1B
39		GND	Ground	1A
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A
42		GND	Ground	1A
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A
45		GND	Ground	1A
46		Reserved	For future use	3A
47		VS1	Module Vendor Specific 1	3A
48		VccRx1	3.3V Power Supply	2A
49		VS2	Module Vendor Specific 2	3A

34	CML-I	Tx3n	Transmitter Inverted Data Input	3B
50		VS3	Module Vendor Specific 3	3A
51		GND	Ground	1A
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A
53	CML-O	Rx7n	Receiver Inverted Data Output	3A
54		GND	Ground	1A
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A
56	CML-O	Rx5n	Receiver Inverted Data Output	3A
57		GND	Ground	1A
58		GND	Ground	1A
59	CML-O	Rx6n	Receiver Inverted Data Output	3A
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A
61		GND	Ground	1A
62	CML-O	Rx8n	Receiver Inverted Data Output	3A
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A
64		GND	Ground	1A
65		NC	No Connect	3A
66		Reserved	For future use	3A
67		VccTx1	3.3V Power Supply	2A
68		Vcc2	3.3V Power Supply	2A
69		Reserved	For Future Use	3A
70		GND	Ground	1A
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A
73		GND	Ground	1A
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A
76		GND	Ground	1A

14. Pin Descriptions

Parameter	Reference	Value	Unit	Note
ESD Immunity	IEC 61000-4-2	8	kV	Contact Discharge
ESD Immunity	IEC 61000-4-2	15	kV	Air Discharge
ESD (HBM model)	JEDEC JESD22-A114-B	1	kV	High-Speed Contacts
ESD (HBM model)	JEDEC JESD22-A114-B	2	kV	Other pins
EMC Immunity	IEC 61000-4-3			
EMI Emission	FCC Class B			

15. Additional Specifications

Application Bit Rate	Baud Rate	Modulation	FEC
478.75 Gb/s	59.84375 GBd	DP-16QAM	CFEC
481.108374 Gb/s	60.1385468 GBd	DP-16QAM	oFEC

16. Additional Specifications

Parameter	Symbol	Min	Max	Unit	Condition
SCL and SDA	VOL	0	0.4	V	IOL(max)=3 mA for fast mode, 20 mA for Fast-mode plus
SCL and SDA	VIL	-0.3	Vcc * 0.3	V	
SCL and SDA	VIH	Vcc * 0.7	Vcc + 0.5	V	
Capacitance for SCL and SDA I/O signal	Ci		14	pF	
Total bus capacitive load for SCL and SDA	Cb		100	pF	For 400 kHz clock rate use 3.0k Ohms Pull-up resistor, max.
Total bus capacitive load for SCL and SDA			200	pF	For 400 kHz clock rate use 1.6k Ohms Pull-up resistor, max.
LPMode, ResetL, ModSelL and ePPS	VIL	-0.3	0.8	V	
LPMode, ResetL, ModSelL and ePPS	VIH	2	Vcc + 0.3	V	
LPMode, ResetL and ModSelL	|Iin|		360	uA	0V<Vin<Vcc
ePPS	|Iin|		Order-specific	uA	0V<Vin<Vcc
IntL	VOL	0	0.4	V	IOL=2.0 mA
IntL	VOH	Vcc – 0.5	Vcc + 0.3	V	10k Ohms pull-up to Host Vcc
ModPrsL	VOL	0	0.4	V	IOL=2.0 mA
ModPrsL	VOH			V	ModPrsL can be implemented as a short-circuit to GND on the module

17. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek