# 400G CFP2 DCO Product Specification

1. Introduction / This document describes the product specifications for 400G CFP2 DCO modules based on probabilistic constellation shaping quadrature amplitude modulation (PS-16QAM) supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. The module can accommodate various client signals such as 100/400 Giga-bit Ethernet (100GbE/400GbE) and Optical Transport channel Uint-4(OTU4). The module will enable the following system performance and features:




## 1. Product Overview

**Features**

- 400G coherent CFP2 DCO with a 200G product option.
- PS-16QAM coherent operation with advanced electronic link equalization.
- Single-channel tunable operation in the extended C-band.
- Operating case temperature: 0 to 70 °C.

**Applications**

## 2. Ordering Information

| Product | Description | Note |
|---|---|---|
| CT-WTCTS400SLHTA00 | Single rate 400Gb/s single channel tunable coherent CFP2 DCO LH, 0 ~ 70℃; | |
| CT-WTCTS200SMRTA00 | Single rate 200Gb/s single channel tunable coherent CFP2 DCO MR, 0 ~ 70℃; | |

## 3. Absolute Maximum Ratings

| Id | Parameter | Condition (1) | Min | Max | Unit |
|---|---|---|---|---|---|
| 1 | Storage Temperature Range | | -40 | 85 | ℃ |
| 2 | Storage Humidity | Relative, no-Condensing | - | 85 | % |
| 3 | Case Temperature Range | | -5 | +70 | ℃ |
| 4 | Power supply | | -0.3 | 3.7 | V |
| 5 | Input power (Optical) | Peak Power | | 5 | dBm |

## 4. Absolute Maximum Ratings

| Id | Parameter | Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | Operating Case Temperature (Top) | | Tcase | 0 | 70 | ℃ |
| 2 | Relative humidity Range | Non-condensing | RH | - | 85 | % |
| 3 | Operating Input Optical Power of Signal | | Psig | -12 | 0 | dBm |
| 4 | Storage Temperature Range | | | -40 | 85 | ℃ |

## 5. Recommended Operating Conditions

| Item | Parameter | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 1 | 3.3V DC Power Supply Voltage | | 3.2 | 3.3 | 3.4 | V |
| 2 | 3.3V DC Power Supply Current | | | | 8 | A |
| 3 | Power Consumption | Low Power | | | 2 | W |
| 4 | Power Consumption @400G PS-16QAM | | | 23 | 25 | W |
| 5 | Power Consumption @200G PS-16QAM | | | 19 | 22 | W |
| 6 | Power Consumption @200G DP- QPSK | | | 21 | 24 | W |
| 7 | Inrush current | Power class 5 & 6 | | | 300 | mA/us |
| 8 | Turn-off current | Power class 5 & 6 | -300 | | | mA/us |
| 9 | Power Supply Noise | DC - 1MHz | | | 2 | % |
| 10 | Power Supply Noise | 1 - 10MHz | | | 3 | % |

## 6. Optical Parameters

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications |
| Serial bit rate | F_bit | 1.250 ± 100ppm | 1.250 ± 100ppm | 1.250 ± 100ppm | 1.250 ± 100ppm | Gb/s |
| Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications |
| Differential peak-to-peak Output Voltage Transmitter enabled | Vodiff | Note 1 | 360 | | 760 | mV |
| Differential peak-to-peak Output Voltage Transmitter disabled | Vdiff_off | Note 1 | | | 110 | mV |
| Rise and Fall Time | tr, tf | 20%-80% | 24 | | 327 | ps |
| Differential Skew | tskw | P to N | | | 25 | ps |
| Deterministic jitter | Dj | Note 2 | | | 0.100 | UIpp |
| Total jitter | Tj | Note 2 | | | 0.240 | UIpp |
| Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications |
| Differential peak-to-peak Input Voltage | Vidiff | | 200 | | 1200 | mV |
| Total Input Jitter Tolerance | Jtol_t | Note 2 | 0.749 | | | UIpp |
| Deterministic Input Jitter Tolerance | Jtol_d | Note 2 | 0.462 | | | UIpp |

## 7. Optical Parameters

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications | Transmitter and Receiver Specifications |
| Serial bit rate | F_bit | 3.125 ± 100ppm | 3.125 ± 100ppm | 3.125 ± 100ppm | 3.125 ± 100ppm | Gb/s |
| Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications | Transmitter Specifications |
| Differential peak-to-peak Output Voltage Transmitter enabled | Vodiff | Note 1 | 360 | | 760 | mV |
| Differential Output Return Loss Max 312.5 MHz < f < 625 MHz | SD22 | Note 2 | -10 | -10 | -10 | dB |
| Differential Output Return Loss Max 625 MHz ≤ f ≤ 3.125 GHz | SD22 | Note 2 | -10 + 10 x log(f/625) | -10 + 10 x log(f/625) | -10 + 10 x log(f/625) | dB |
| Deterministic jitter | Dj | Note 3 | | | 0.17 | UIpp |
| Total jitter | Tj | Note 3 | | | 0.35 | UIpp |

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications | Receiver Specifications |
| Differential peak-to-peak Input Voltage | Vidiff | | 200 | | 1200 | mV |
| Differential Input Return Loss 100 MHz ≤ f ≤ 2.5 GHz | SD11_d | Note 4 | | | -10 | dB |
| Common-mode Input Return Loss 100 MHz ≤ f ≤ 2.5 GHz | SD11_c | Note 4 | | | -6 | dB |
| Total Input Jitter Tolerance | Jtol_t | Note 3 | 0.65 | | | UIpp |
| Deterministic Input Jitter Tolerance | Jtol_d | Note 3 | 0.37 | | | UIpp |

# 8. Optical Parameters

| Id | Parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 1 | Transmitter Frequency Range | 193.7 | 191.3 | 196.10 | THz | Frequency range over which the specifications hold unless noted otherwise. |
| 2 | Channel Spacing | 75 | | | GHz | Flex Grid |
| 3 | Frequency Stability | | -1.8 | 1.8 | GHz | |
| 4 | Frequency Offset | | -1.8 | 1.8 | GHz | |
| 5 | Frequency Fine Tuning Range | | -6.0 | 6.0 | GHz | |
| 6 | Fine Tuning Resolution | 100 | | | MHz | |
| 7 | Channel Tuning Speed | | | 60 | s | |
| 8 | Line Width | | 100 | 300 | kHz | FWHM |
| 9 | SMSR (Side mode suppression Ratio) | 37 | 36 | | dB | Measured over +/- 2.5nm range around the target frequency with 0.06nm RBW without modulation. |
| 10 | Transmitter output power range | 0 | -5 | 5 | dBm | Transmitter output is settable in steps of 0.1 dB at any power level within the specified frequency range |
| 11 | Output power stability | | -0.5 | 0.5 | dB | Output power change over temperature and over time, measured over 10ms second intervals. |
| 12 | Output power accuracy | | -1 | 1 | dB | Difference between the set value and actual value over aging. |

| Id | Parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 13 | Transmitter turn-up time from warm start | 10 | - | 15 | ms | Module is in Ready state. The maximum transmitter turn-up time is counted from de-assert the Tx_disable Pin to full Tx turn-up. |
| 14 | Transmitter laser disable time | 1 | - | 3 | ms | Tx is in full turn-up state. The maximum transmitter turn-off time is counted from assert Tx_disable pin |
| 15 | Transmitter turn-up time from cold start | | - | 160 | s | Module is in Low_Power mode. The maximum Tx turn-up time is counted from de-assert the Low_power pin and Tx_disable pin to full Tx turn-up. |
| 16 | Transmitter OSNR | | 34 | | dB/0.1nm | Noise Power is the max power measured in frequency range 191.275THz .... fs - 75GHz and fs + 75GHz 196.125THz and referenced to 12.5GHz noise bandwidth fs: target operating frequency |
| 17 | Transmitter optical return loss | | 27 | - | dB | |
| 18 | Transmitter output power with TX disabled | | | -40 | dBm | E.g., max output power when changing laser frequency. |
| 19 | Transmitter polarization dependent power | | | 1 | dB | Power deference between X and Y polarization |

# 9. Optical Parameters

| Pin Number | Name of Pin | Structure | Logic | Description / Connection |
|---|---|---|---|---|
| Pin Number | Name of Pin | (Input/Output) | Logic | Description / Connection |
| 1 | GND | GND | Ground | |
| 2 | OHIO_RDn | O | CML | OHIO output: Differential 100Ω built-in |
| 3 | OHIO_RDp | O | CML | OHIO output |
| 4 | GND | GND | Ground | |
| 5 | OHIO_TDn | I | CML | OHIO input: Differential 100Ω built-in |
| 6 | OHIO_TDp | I | CML | OHIO input |
| 7 | 3.3V GND | PWR_GND | Ground | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |

| Pin Number | Name of Pin | Structure | Logic | Description / Connection |
|---|---|---|---|---|
| 8 | 3.3V GND | PWR_GND | Ground | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 9 | 3.3V | PWR | Power | 3.3V Module Supply Voltage |
| 10 | 3.3V | PWR | Power | 3.3V Module Supply Voltage |
| 11 | 3.3V | PWR | Power | 3.3V Module Supply Voltage |
| 12 | 3.3V | PWR | Power | 3.3V Module Supply Voltage |
| 13 | 3.3V GND | PWR_GND | Ground | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 14 | 3.3V GND | PWR_GND | Ground | 3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground |
| 15 | VND_IO_A | I/O | LVCMOS | TXD0 of Uart0 (For FPGA: Module to PC) |
| 16 | VND_IO_B | I/O | LVCMOS | RXD0 of Uart0 (For FPGA: PC to Module) |
| 17 | PRG_CNTL1 | I | LVCMOS w/PUR | Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled or not used |
| 18 | PRG_CNTL2 | I | LVCMOS w/PUR | Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC: ≤18W or not used |
| 19 | PRG_CNTL3 | I | LVCMOS w/PUR | Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC:≤18W or not used |
| 20 | PRG_ALRM1 | O | LVCMOS | Programmable Alarm 1; MSA Default “H” = HIPWR_ON |
| 21 | PRG_ALRM2 | O | LVCMOS | Programmable Alarm 2; MSA Default “H” = MOD_READY |
| 22 | PRG_ALRM3 | O | LVCMOS | Programmable Alarm 3; MSA Default “H” = MOD_FAULT |
| 23 | GND | GND | Ground | |
| 24 | TX_DIS | I | LVCMOS w/PUR | Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled |

| Pin Number | Name of Pin | Structure | Logic | Description / Connection |
|---|---|---|---|---|
| 25 | RX_LOS | O | LVCMOS | Receiver Loss of Optical Signal, "1": low optical signal, |

## 10. Optical Parameters

| #Pin | Name | Description |
|---|---|---|
| #Pin | 8x56G PAM4 | Description |
| 104 | GND | Ground |
| 103 | TX4n | Transmitter lane 4 |
| 102 | TX4p | Transmitter lane 4 |
| 101 | GND | Ground |
| 100 | TX3n | Transmitter lane 3 |
| 99 | TX3p | Transmitter lane 3 |
| 98 | GND | Ground |
| 97 | TX2n | Transmitter lane 2 |
| 96 | TX2p | Transmitter lane 2 |
| 95 | GND | Ground |
| 94 | TX5n | Transmitter lane 5 |
| 93 | TX5p | Transmitter lane 5 |
| 92 | GND | Ground |
| 91 | TX6n | Transmitter lane 6 |
| 90 | TX6p | Transmitter lane 6 |
| 89 | GND | Ground |
| 88 | TX1n | Transmitter lane 1 |
| 87 | TX1p | Transmitter lane 1 |
| 86 | GND | Ground |
| 85 | TX0n | Transmitter lane 0 |
| 84 | TX0p | Transmitter lane 0 |
| 83 | GND | Ground |
| 82 | TX7n | Transmitter lane 7 |
| 81 | TX7p | Transmitter lane 7 |
| 80 | GND | Ground |
| 79 | N.C. | N.C |
| 78 | N.C. | N.C |
| 77 | GND | Ground |
| 76 | RX4n | Receiver lane 4 |
| 75 | RX4p | Receiver lane 4 |
| 74 | GND | Ground |
| 73 | RX3n | Receiver lane 3 |
| 72 | RX3p | Receiver lane 3 |

## 11. Additional Specifications

| Applications | Client-Side type | Client I/F mode | Client lane rate (GBd) | Note |
|---|---|---|---|---|
| 400G | 1*400G | 1*400GAUI-8 | 8*26.5625 | |
| 400G | 4*100G | 4*100GAUI-2 | 4*(2*26.5625) | |
| 400G | 4*OTU4 | 4*OTL4.2 | 4*(2*27.9525) | |
| 400G | OTUC4 | 4*FOIC1.2 | 4*(2*27.9524) | |
| 200G | 2*100G | 2*CAUI-4 w/o FEC | 2*(4*25.78125) | |
| 200G | 2*100G | 2*CAUI-4 w/ RS FEC | 2*(4*25.78125) | |
| 200G | 2*OTU4 | 2*OTL4.4 | 2*(4*27.9525) | |

## 12. Additional Specifications

| Application | Host Frame | Host Data Bit Rate(Gbps) | Offset(ppm) | Singal |
|---|---|---|---|---|
| 400G | 1*400GAUI-8 | 1*425 | 100 | Ethernet class |
| 400G | 4*100GAUI-2 | 4*106.25 | 100 | Ethernet class |
| 400G | 4*OTL4.2 | 4*111.81 | 20 | |
| 400G | 4*FOIC1.2 | 4*111.81 | 20 | |
| 200G | 2*CAUI-4 w/o FEC | 2*103.125 | 100 | Ethernet class |
| 200G | 2*CAUI-4 w/ RS FEC | 2*103.125 | 100 | Ethernet class |
| 200G | 2*OTL4.4 | 2*111.81 | 20 | |

## 13. Additional Specifications

| Id | Application | Modulation | FEC Type | Lane Baud | Grid | OSNR | Note |
|---|---|---|---|---|---|---|---|
| 1 | 400G | PS-16QAM | SDFEC | 67GBd | 75GHz | 21dB | |
| 2 | 200G | PS-16QAM | SDFEC | 41.08GBd | 50GHz | 16dB | |
| 3 | 200G | DP-QPSK | SDFEC | 64.01GBd | 75GHz | 14dB | |

## 14. Additional Specifications

| Id | parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 1 | Receiver Frequency Range | 193.7 | 191.3 | 196.10 | THz | C band 75GHz ITU-T grid. |
| 2 | Input power range | | -12 | 0 | dBm | Signal power of the selected channel |
| 3 | OSNR Sensitivity | 21 | | 22 | dB/0.1nm | At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above. |

| Id | parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 4 | Receiver Sensitivity | | | -20 | dBm | Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled |
| 5 | Los assert | | | -28 | dBm | |
| 6 | Los de-assert | | | -25 | dBm | |
| 7 | Los hysteresis | | | 3 | dB | |
| 8 | CD Tolerance | | | 36000 | ps/nm | With less than 0.5dB OSNR penalty at FEC threshold. |
| 9 | DGD tolerance | | 70 | | ps | DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold; |
| 10 | PDL tolerance | | 3.5 | | dB | PDL tolerance under the following conditions: PDL applied before noise loading; Change in SOP is <=1rad/millisecond; With additional 1.5dB OSNR penalty |
| 11 | Tolerance to change in SOP | | 100 | - | rad/ms | Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold. |
| 12 | Input power transient tolerance | | 3 | - | dB | Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50μs or slower. |
| 13 | Input power reading accuracy | | -2 | 2 | dB | The module reports the actual power as received by the module. |
| 14 | Optical Return Loss | | 27 | | dB | |
| 15 | Receiver turn-up time from cold start | | - | 160 | Seconds | Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready. |
| 16 | RX LOS Assert time | | | 3 | ms | Assert Time of Receiver Loss of Signal |
| 17 | RX LOS De- assert time | | | 3 | ms | De-assert Time of Receiver Loss of Signal |

## 15. Additional Specifications

| Id | parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 1 | Receiver Frequency Range | 193.7 | 191.3 | 196.10 | THz | C band 75GHz ITU-T grid. |
| 2 | Input power range | | -18 | 0 | dBm | Signal power of the selected channel |
| 3 | OSNR Sensitivity | 16 | | 17 | dB/0.1nm | At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above. |
| 4 | Receiver Sensitivity | | | -21 | dBm | Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled |
| 5 | Los assert | | | -28 | dBm | |
| 6 | Los de-assert | | | -25 | dBm | |
| 7 | Los hysteresis | | | 3 | dB | |
| 8 | CD Tolerance | | | 40000 | ps/nm | With less than 0.5dB OSNR penalty at FEC threshold. |
| 9 | DGD tolerance | | 70 | | ps | DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold; |
| 10 | PDL tolerance | | 3.5 | | dB | PDL tolerance under the following conditions: PDL applied before noise loading; Change in SOP is <=1rad/millisecond; With additional 1.5dB OSNR penalty |
| 11 | Tolerance to change in SOP | | 100 | - | rad/ms | Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold. |
| 12 | Input power transient tolerance | | 3 | - | dB | Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50μs or slower. |
| 13 | Input power reading accuracy | | -2 | 2 | dB | The module reports the actual power as received by the module. |
| 14 | Optical Return Loss | | 27 | | dB | |

| Id | parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 15 | Receiver turn-up time from cold start | | - | 160 | Seconds | Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready. |
| 16 | RX LOS Assert time | | | 3 | ms | Assert Time of Receiver Loss of Signal |
| 17 | RX LOS De- assert time | | | 3 | ms | De-assert Time of Receiver Loss of Signal |

## 16. Additional Specifications

| Id | parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 1 | Receiver Frequency Range | 193.7 | 191.3 | 196.10 | THz | C band 75GHz ITU-T grid. |
| 2 | Input power range | | -18 | 0 | dBm | Signal power of the selected channel |
| 3 | OSNR Sensitivity | 14 | | 15 | dB/0.1nm | At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above. |
| 4 | Receiver Sensitivity | | | -21 | dBm | Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled |
| 5 | Los assert | | | -28 | dBm | |
| 6 | Los de-assert | | | -25 | dBm | |
| 7 | Los hysteresis | | | 3 | dB | |
| 8 | CD Tolerance | | | 40000 | ps/nm | With less than 0.5dB OSNR penalty at FEC threshold. |
| 9 | DGD tolerance | | 70 | | ps | DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold; |
| 10 | PDL tolerance | | 3.5 | | dB | PDL tolerance under the following conditions: PDL applied before noise loading; Change in SOP is <=1rad/millisecond; With additional 1.5dB OSNR penalty |
| 11 | Tolerance to change in SOP | | 100 | - | rad/ms | Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold. |

| Id | parameter | Typ | Min | Max | Unit | Condition/comments |
|---|---|---|---|---|---|---|
| 12 | Input power transient tolerance | | 3 | - | dB | Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50μs or slower. |
| 13 | Input power reading accuracy | | -2 | 2 | dB | The module reports the actual power as received by the module. |
| 14 | Optical Return Loss | | 27 | | dB | |
| 15 | Receiver turn-up time from cold start | | - | 160 | Seconds | Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready. |
| 16 | RX LOS Assert time | | | 3 | ms | Assert Time of Receiver Loss of Signal |
| 17 | RX LOS De- assert time | | | 3 | ms | De-assert Time of Receiver Loss of Signal |

# 17. Additional Specifications

| Pin Number | Name of Pin | | Pin Number | Name of Pin |
|---|---|---|---|---|
| 1 | GND | | 104 | GND |
| 2 | OHIO_RD0n | | 103 | TX4n |
| 3 | OHIO_RD0p | | 102 | TX4p |
| 4 | GND | | 101 | GND |
| 5 | OHIO_TD0n | | 100 | TX3n |
| 6 | OHIO_TD0p | | 99 | TX3p |
| 7 | 3.3V GND | | 98 | GND |
| 8 | 3.3V GND | | 97 | TX2n |
| 9 | 3.3V | | 96 | TX2p |
| 10 | 3.3V | | 95 | GND |
| 11 | 3.3V | | 94 | TX5n |
| 12 | 3.3V | | 93 | TX5p |
| 13 | 3.3V GND | | 92 | GND |
| 14 | 3.3V GND | | 91 | TX6n |
| 15 | VND_IO_A | | 90 | TX6p |
| 16 | VND_IO_B | | 89 | GND |

| Pin Number | Name of Pin | | Pin Number | Name of Pin |
|---|---|---|---|---|
| 17 | PRG_CNTL1 | | 88 | TX1n |
| 18 | PRG_CNTL2 | | 87 | TX1p |
| 19 | PRG_CNTL3 | | 86 | GND |
| 20 | PRG_ALRM1 | | 85 | TX0n |
| 21 | PRG_ALRM2 | | 84 | TX0p |
| 22 | PRG_ALRM3 | | 83 | GND |
| 23 | GND | | 82 | TX7n |
| 24 | TX_DIS | | 81 | TX7p |
| 25 | RX_LOS | | 80 | GND |
| 26 | MOD_LOPWR | | 79 | N.C. |
| 27 | MOD_ABS | | 78 | N.C. |
| 28 | MOD_RSTn | | 77 | GND |
| 29 | GLB_ALRMn | | 76 | RX4n |
| 30 | GND | | 75 | RX4p |
| 31 | MDC | | 74 | GND |
| 32 | MDIO | | 73 | RX3n |
| 33 | PRTADR0 | | 72 | RX3p |
| 34 | PRTADR1 | | 71 | GND |
| 35 | PRTADR2 | | 70 | RX2n |
| 36 | VND_IO_C | | 69 | RX2p |
| 37 | VND_IO_D | | 68 | GND |
| 38 | VND_IO_E | | 67 | RX5n |
| 39 | 3.3V GND | | 66 | RX5p |
| 40 | 3.3V GND | | 65 | GND |
| 41 | 3.3V | | 64 | RX6n |
| 42 | 3.3V | | 63 | RX6p |
| 43 | 3.3V | | 62 | GND |
| 44 | 3.3V | | 61 | RX1n |
| 45 | 3.3V GND | | 60 | RX1p |
| 46 | 3.3V GND | | 59 | GND |
| 47 | OHIO_TD1n | | 58 | RX0n |
| 48 | OHIO_TD1p | | 57 | RX0p |
| 49 | GND | | 56 | GND |
| 50 | OHIO_RD1n | | 55 | RX7n |
| 51 | OHIO_RD1p | | 54 | RX7p |
| 52 | GND | | 53 | GND |

## 18. Additional Specifications

| | | | | "0": normal condition |
|---|---|---|---|---|
| 26 | MOD_LOPWR | I | LVCMOS w/PUR | Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled |
| 27 | MOD_ABS | O | GND | Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host |
| 28 | MOD_RSTn | I | LVCMOS w/PUR | Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module |
| 29 | GLB_ALRMn | O | LVCMOS | Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host |
| 30 | GND | GND | Ground | |
| 31 | MDC | I | 1.2V LVCMOS | Management Data Clock (electrical specs as per IEEE Std 802.3- 2012) |
| 32 | MDIO | I/O | 1.2V LVCMOS | Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012) |
| 33 | PRTADR0 | I | 1.2V LVCMOS | MDIO Physical Port Address bit 0 |
| 34 | PRTADR1 | I | 1.2V LVCMOS | MDIO Physical Port Address bit 1 |
| 35 | PRTADR2 | I | 1.2V LVCMOS | MDIO Physical Port Address bit 2 |
| 36 | VND_IO_C | I/O | LVCMOS | TMS/SWDIO (PC to Module or Module to PC) |
| 37 | VND_IO_D | I | LVCMOS | TCK/SWDCK (PC to Module) |
| 38 | VND_IO_E | I/O | LVCMOS | TXD1 of Uart1 (Module to PC) |
| 39 | 3.3V GND | PWR_GND | Ground | Power Ground. Internally connected to logic GND. power supply return path. |
| 40 | 3.3V GND | PWR_GND | Ground | Power Ground. Internally connected to logic GND. power supply return path. |
| 41 | 3.3V | PWR | Power | 3.3V power supply |
| 42 | 3.3V | PWR | Power | 3.3V power supply |
| 43 | 3.3V | PWR | Power | 3.3V power supply |
| 44 | 3.3V | PWR | Power | 3.3V power supply |
| 45 | 3.3V GND | PWR_GND | Ground | Power Ground. Internally connected to logic GND. power supply return path. |

| | | | | "0": normal condition |
|---|---|---|---|---|
| 46 | 3.3V GND | PWR_GND | Ground | Power Ground. Internally connected to logic GND. power supply return path. |
| 47 | OHIO_REFCLKn | I | CML | OHIO ref clk input,100MHz, ±100 ppm，100-1200mVppd |
| 48 | OHIO_REFCLKp | I | CML | OHIO ref clk input,Differential 100Ω built-in |
| 49 | GND | GND | Ground | Module Ground. Logic and power return path |
| 50 | TX_MCKLn | O | CML | TX lineside monitor clock |
| 51 | TX_MCKLn | O | CML | TX lineside monitor clock |
| 52 | GND | GND | Ground | Module Ground. Logic and power return path |

## 19. Additional Specifications

| 71 | GND | Ground |
|---|---|---|
| 70 | RX2n | Receiver lane 2 |
| 69 | RX2p | Receiver lane 2 |
| 68 | GND | Ground |
| 67 | RX5n | Receiver lane 5 |
| 66 | RX5p | Receiver lane 5 |
| 65 | GND | Ground |
| 64 | RX6n | Receiver lane 6 |
| 63 | RX6p | Receiver lane 6 |
| 62 | GND | Ground |
| 61 | RX1n | Receiver lane 1 |
| 60 | RX1p | Receiver lane 1 |
| 59 | GND | Ground |
| 58 | RX0n | Receiver lane 0 |
| 57 | RX0p | Receiver lane 0 |
| 56 | GND | Ground |
| 55 | RX7n | Receiver lane 7 |
| 54 | RX7p | Receiver lane 7 |
| 53 | GND | Ground |

## 20. Additional Specifications

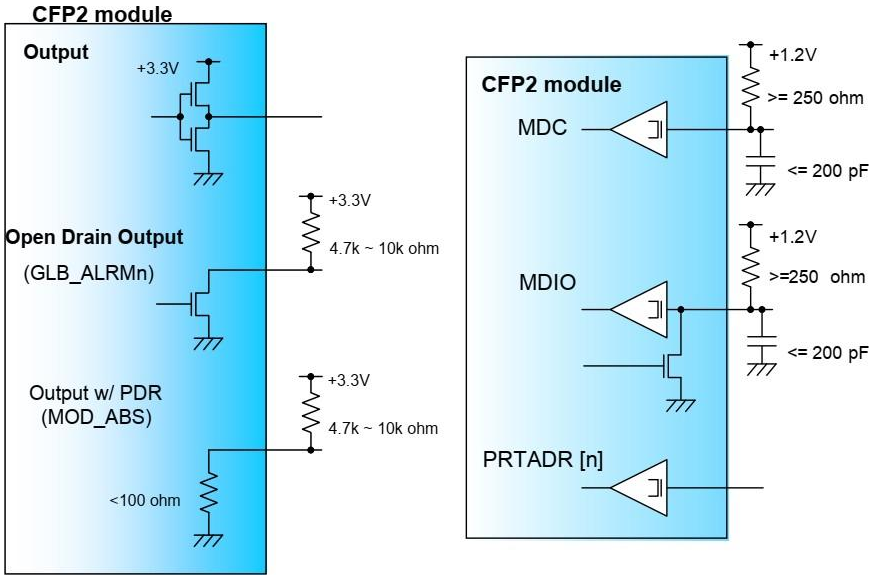
| SerDes Lanes | 1*400G | 4*100G | 2*100G |
|---|---|---|---|
| SerDes Lanes | 1*400GAUI-8 (PAM4) | 4*100GAUI-2 4*OTL4.2 (PAM4) | 2*100G CAUI-4 2*OTL4.4 (NRZ) |
| SerDes Lanes | Interface - CH[x,y] | Interface - CH[x,y] | Interface - CH[x,y] |
| Tx7[p,n];Rx7[p,n] | CH4.1 | CH4.4 | CH2.2 |

| SerDes Lanes | 1*400G | 4*100G | 2*100G |
|---|---|---|---|
| Tx6[p,n];Rx6[p,n] | CH4.1 | CH4.4 | CH2.2 |
| Tx5[p,n];Rx5[p,n] | CH4.1 | CH4.3 | CH2.2 |
| Tx4[p,n];Rx4[p,n] | CH4.1 | CH4.3 | CH2.2 |
| Tx3[p,n];Rx3[p,n] | CH4.1 | CH4.2 | CH2.1 |
| Tx2[p,n];Rx2[p,n] | CH4.1 | CH4.2 | CH2.1 |
| Tx1[p,n];Rx1[p,n] | CH4.1 | CH4.1 | CH2.1 |
| Tx0[p,n];Rx0[p,n] | CH4.1 | CH4.1 | CH2.1 |

# 21. Additional Specifications

| Glossary | Info. |
|---|---|
| ADC | Analog to Digital Converter |
| AGC | Automatic Gain Control |
| BS | Beam Splitter |
| CMRR | Common Mode Rejection Ratio |
| DSP | Digital Signal Processor |
| IA | Implementation Agreement |
| LO | Local Oscillator |
| MGC | Manual Gain Control |
| MPD | Monitor Photodiode |
| MSA | Multi-Source Agreement |
| OIF | Optical Internetworking Forum |
| PBS | Polarization Beam Splitter |
| PCB | Printed Circuit Board |
| DP-16QAM | Dual Polarization Quadrature Amplitude Modulation |
| PS-16QAM | Probabilistic Constellation Shaping Quadrature Amplitude Modulation |
| OUT4 | Optical Transport channel Uint-4 |
| OTUCn | Optical Transport Unit Cn |

## 22. Technical Figure 1




## 23. Revision History

| Version | Date | Description | Prepared by |
|---|---|---|---|
| V6 | 2025 | Unified WincoTek datasheet format | WincoTek |
| V6.1 | 2026-10-23 | Engineering and format review | WincoTek |