WTOS400-SR4-100C

OSFP 400Gb/s MPO SR4 100m DDM /
PRODUCT FEATURES

Data Rate 425	Wavelength 850



1. Product Overview

Features

- Data rate up to 425Gbps (4xPAM4 53.125 GBd)
- High speed I/O electrical interface (400GAUI-4)
- Support 5 applications:
- 400GBASE-SR4
- 200GBASE-SR4
- 100GBASE-SR4
- 2x 200GBASE-SR2
- 4x 100GBASE-SR1
- Compliant to OSFP MSA Rev5.0
- Maximum link length of 60m on OM3 or 100m on OM4
- 4x VCSEL arrays and 4x PIN PD arrays
- Optical connector: MPO -12(APC)

Applications

- 400GBASE-SR4 400G Ethernet
- Data center

2. Ordering Information

Part NO.	Bit Rate (Gbps)	Laser (nm)	Distance(m)	Media	DDMI	Connector	Temp（℃）
WTOS400-SR4-100C	425	850	100 (OM4)	multi-mode fiber	YES	MPO-12（APC）	0~70

3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Storage Temperature	TS	-40		85	ºC	
Storage Ambient Humidity	HA	15		85	%	
Maximum Supply Voltage	VCC	-0.5		3.6	V	
Receiver damage Threshold，per lane		5			dBm	
Lead Soldering Temperature/Time	TSOLD			260/10	ºC/sec	1
Lead Soldering Temperature/Time	TSOLD			360/10	ºC/sec	2

4. Recommended Operating Conditions

Data Rate Spcifications	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR			66	mV	10Hz~10MHz
Instantaneous peak current at high power enable	Icc_ip			3200	mA	
Sustained peak current at high power enable	Icc_sp			2666	mA	
Supply steady state Current	Icc			2552	mA	Steady state
Operating Case Temperature	Tc	0		70	℃	
Link distance on OM4 MMF	d			100	meters	

5. Recommended Operating Conditions

Parameter	Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Transmitter(per lane)	Transmitter(per lane)	Transmitter(per lane)	Transmitter(per lane)	Transmitter(per lane)	Transmitter(per lane)	Transmitter(per lane)	Transmitter(per lane)
Channel data rate	Channel data rate	FDC	106.25	106.25	106.25	Gb/s	
Signaling rate	Signaling rate	FSG	53.125	53.125	53.125	GBd	PAM4
Signal speed variation from nominal	Signal speed variation from nominal	⊿FSG	-100		+100	Ppm	
Center Wavelength	Center Wavelength	λC	840		860	nm	
RMS Spectral Width	RMS Spectral Width	σ			0.6	nm	1
Average Launch power， each lane	Average Launch power， each lane		-4.6		4	dBm	
Outer Optical Modulation Amplitude (OMA outer), each lane	max(TECQ, TDECQ) ≤ 1.8dB		max [-2.6 , max(TECQ,TDECQ) – 4.4]	max [-2.6 , max(TECQ,TDECQ) – 4.4]	max [-2.6 , max(TECQ,TDECQ) – 4.4]	dBm	
Outer Optical Modulation Amplitude (OMA outer), each lane	1.8 < max (TECQ, TDECQ) ≤ 4.4dB		max [-2.6 , max(TECQ,TDECQ) – 4.4]	max [-2.6 , max(TECQ,TDECQ) – 4.4]	max [-2.6 , max(TECQ,TDECQ) – 4.4]	dBm	
Transmitter and dispersion eye closure for PAM4, each lane	Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			4.4	dB	
Transmitter eye closure for PAM4 (TECQ), each lane	Transmitter eye closure for PAM4 (TECQ), each lane	TECQ			4.4	dB	
Transmitter power excursion, each lane	Transmitter power excursion, each lane				2.3		
Average Optical Output Power of Off Transmitter, each lane	Average Optical Output Power of Off Transmitter, each lane	Poff			-30	dBm	

Parameter	Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Extinction Ratio, each lane	Extinction Ratio, each lane	ER	2.5			dB	
Optical return loss tolerance	Optical return loss tolerance				14	dB	
Encircled flux	Encircled flux		≥86% at 19um ≤30% at 4.5um	≥86% at 19um ≤30% at 4.5um	≥86% at 19um ≤30% at 4.5um		2
Receiver(per lane)	Receiver(per lane)	Receiver(per lane)	Receiver(per lane)	Receiver(per lane)	Receiver(per lane)	Receiver(per lane)	Receiver(per lane)
Damage threshold	Damage threshold		5			dBm	3
Average receive power, each lane	Average receive power, each lane		–6.4		4.0	dBm	4
Receive power (OMA outer), each lane	Receive power (OMA outer), each lane				3.5	dBm	
Receiver reflectance	Receiver reflectance				-15	dB	
Receiver sensitivity(OMA outer), each lane	TECQ ≤ 1.8dB				-4.6	dBm	5 Figure 2
Receiver sensitivity(OMA outer), each lane	1.8 < TECQ ≤ 4.4dB				-6.4+ TECQ	dBm	5 Figure 2
Receiver Loss of Signal Indicator Assert Level	Receiver Loss of Signal Indicator Assert Level	LOSA	-15			dBm	
Receiver Loss of Signal Indicator De-assert Level	Receiver Loss of Signal Indicator De-assert Level	LOSD			-7.5	dBm	
Hysteresis	Hysteresis	LOSH	0.5		5	dB	
Stressed receiver sensitivity (OMA outer), each lane	Stressed receiver sensitivity (OMA outer), each lane				-2	dBm	5, 6
Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:	Conditions of stressed receiver sensitivity test:
Stressed eye closure for PAM4(SECQ), lane under test	Stressed eye closure for PAM4(SECQ), lane under test	Stressed eye closure for PAM4(SECQ), lane under test	4.4	4.4	4.4	dB	
OMA outer of each aggressor lane	OMA outer of each aggressor lane	OMA outer of each aggressor lane	3.5	3.5	3.5	dBm	

6. Optical Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Supply Voltage	VCC	3.135		3.465	V	
Power Dissipation	Pd			8	W	
Transmitter(per Lane)	Transmitter(per Lane)	Transmitter(per Lane)	Transmitter(per Lane)	Transmitter(per Lane)	Transmitter(per Lane)	Transmitter(per Lane)
Signaling rate per lane (range)	-	-100ppm	53.125	+100ppm	GBd	PAM4
Differential data output swing	-	300		900	mVpp	
Eye height	-	15			mV	

Parameter	Symbol	Min.	Typ.	Max.	Unit	Ref.
Vertical eye closure	VEC			12	dB	
Common-mode to differential-mode return loss	RLdc	Equation (120G-1)			dB	2
Effective return loss	ERL	8.5			dB	
Differential termination mismatch	-			10	%	
Transition time (20% to 80%)	Tt	8.5			ps	
Receiver (per Lane)	Receiver (per Lane)	Receiver (per Lane)	Receiver (per Lane)	Receiver (per Lane)	Receiver (per Lane)	Receiver (per Lane)
Signaling rate, each lane (range)	-	-100ppm	53.125	+100ppm	GBd	at TP1
Differential pk-pk input voltage tolerance	-	750			mV	at TP1a
Differential-mode to common-mode return loss	RLcd	Equation (120G-1)			dB	2 at TP1
Effective return loss	ERL	7.3			dB	at TP1
Differential termination mismatch	-			10	%	at TP1
Vertical eye closure	-			12	dB	at TP1
Transition Time	Tt	10			ps	at TP1

7. Pin Descriptions

Pin	Name	Logic	Description	Plug Sequence	Notes
1	GND		Ground	1	
2	Tx2p	CML-I	Receiver Data Non-Inverted	3	
3	Tx2n	CML-I	Receiver Data Inverted	3	
4	GND		Ground	1	
5	Tx4p	CML-I	Receiver Data Non-Inverted	3	
6	Tx4n	CML-I	Receiver Data Inverted	3	
7	GND		Ground	1	
Pin	Name	Logic	Description	Plug Sequence	Notes
8	Tx6p	CML-I	Receiver Data Non-Inverted	3	
9	Tx6n	CML-I	Receiver Data Inverted	3	
10	GND		Ground	1	
11	TX8p	CML-I	Receiver Data Non-Inverted	3	

Pin	Name	Logic	Description	Plug Sequence	Notes
12	TX8n	CML-I	Receiver Data Inverted	3	
13	GND		Ground	1	
14	SCL	LVCMOS- I/O	2-wire Serial interface clock	3	
15	VCC		+3.3V Power	2	
16	VCC		+3.3V Power	2	
17	LPWn/PRSn	Multi- Level	Low-Power Mode / Module Present	3	1A
18	GND		Ground	1	
19	RX7n	CML-O	Receiver Data Inverted	3	
20	RX7p	CML-O	Receiver Data Non-Inverted	3	
21	GND		Ground	1	
22	RX5n	CML-O	Receiver Data Inverted	3	
23	RX5p	CML-O	Receiver Data Non-Inverted	3	
24	GND		Ground	1	
25	RX3n	CML-O	Receiver Data Inverted	3	
26	RX3p	CML-O	Receiver Data Non-Inverted	3	
27	GND		Ground	1	
28	RX1n	CML-O	Receiver Data Inverted	3	
29	RX1p	CML-O	Receiver Data Non-Inverted	3	
30	GND		Ground	1	
31	GND		Ground	1	
32	RX2p	CML-O	Receiver Data Non-Inverted	3	
33	RX2n	CML-O	Receiver Data Inverted	3	
34	GND		Ground	1	
35	RX4p	CML-O	Receiver Data Non-Inverted	3	
Pin	Name	Logic	Description	Plug Sequence	Notes
36	RX4n	CML-O	Receiver Data Inverted	3	
37	GND		Ground	1	
38	RX6p	CML-O	Receiver Data Non-Inverted	3	
39	RX6n	CML-O	Receiver Data Inverted	3	
40	GND		Ground	1	

Pin	Name	Logic	Description	Plug Sequence	Notes
41	RX8p	CML-O	Receiver Data Non-Inverted	3	
42	RX8n	CML-O	Receiver Data Inverted	3	
43	GND		Ground	1	
44	INT/RSTn	Multi- Level	Module Interrupt / Module Reset	3	1B
45	VCC		+3.3V Power	2	
46	VCC		+3.3V Power	2	
47	SDA	LVCMOS- I/O	2-wire Serial interface data	3	
48	GND		Ground	1	
49	TX7n	CML-I	Transmitter Data Inverted	3	
50	TX7p	CML-I	Transmitter Data Non-Inverted	3	
51	GND		Ground	1	
52	TX5n	CML-I	Transmitter Data Inverted	3	
53	TX5p	CML-I	Transmitter Data Non-Inverted	3	
54	GND		Ground	1	
55	TX3n	CML-I	Transmitter Data Inverted	3	
56	TX3p	CML-I	Transmitter Data Non-Inverted	3	
57	GND		Ground	1	
58	TX1n	CML-I	Transmitter Data Inverted	3	
59	TX1p	CML-I	Transmitter Data Non-Inverted	3	
60	GND		Ground	1	

8. Additional Specifications

Parameter	Nominal	Min	Max	Unit	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_INT	2.500	2.475	2.525	Volts	Precision voltage reference for H_INT
M_Vref_RSTn	1.250	1.238	1.263	Volts	Precision voltage reference for M_RSTn
R1	68k	66k	70k	Ohms	Recommend 68.1k ohms 1% resistor
R2	5k	4.9k	5.1k	Ohms	Recommend 4.99k ohms 1% resistor

Parameter	Nominal	Min	Max	Unit	Note
R3	8k	7.8k	8.2k	Ohms	Recommend 8.06k ohms 1% resistor
V_INT/RSTn_1	0.000	0.000	1.000	Volts	INT/RSTn voltage for No Module
V_INT/RSTn_2	0.000	0.000	1.000	Volts	INT/RSTn voltage for Module installed, H_RSTn=Low
V_INT/RSTn_3	1.900	1.500	2.250	Volts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=Low
V_INT/RSTn_4	3.000	2.750	3.465	V0lts	INT/RSTn voltage for Module installed, H_RSTn=High, M_INT=High

9. Additional Specifications

Parameter	Nominal	Min	Max	Unit	Note
Host VCC	3.300	3.135	3.465	Volts	VCC voltage on the Host
H_Vref_PRSn	2.500	2.475	2.525	Volts	Precision voltage reference for H_PRSn
M_Vref_LPWn	1.250	1.238	1.263	Volts	Precision voltage reference for M_LPWn
R1	25k	24.5k	25.5k	Ohms	Recommend 24.9k ohms 1% resistor
R2	15k	14.7k	15.3k	Ohms	Recommend 15k ohms 1% resistor
R3	10k	9.8k	10.2k	Ohms	Recommend 10k ohms 1% resistor
V_INT/RSTn_1	0.950	0.000	1.100	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=Low
V_INT/RSTn_2	1.700	1.400	2.250	Volts	LPWn/PRSn voltage for Module installed, H_LPWn=High
V_INT/RSTn_3	3.300	2.750	3.465	Volts	LPWn/PRSn voltage for No Module

10. Management Interface Timing

Parameter	Symbol	Fast Mode (400 kHz)	Fast Mode (400 kHz)	Unit	Conditions
Parameter	Symbol	Min	Max	Unit	Conditions
Clock Frequency	fSCL	0	400	kHz	
Clock Pulse Width Low	tLOW	1.3		µs	
Clock Pulse Width High	tHIGH	0.6		µs	

Parameter	Symbol	Fast Mode (400 kHz)	Fast Mode (400 kHz)	Unit	Conditions
Time bus free before new transmission can start	tBUF	20		μs	Between STOP and START and between ACK and ReStart
START Hold Time	tHD.STA	0.6		μs	The delay required between SDA becoming low and SCL starting to go low in a START
START Setup Time	tSU.STA	0.6		μs	The delay required between SCL becoming high and SDA starting to go low in a START
Data In Hold Time	tHD.DAT	0		μs	
Data In Setup Time	tSU.DAT	0.1		μs	
Input Rise Time	tR		300	ns	From (VIL,MAX=0.3*Vcc) to (VIH, MIN=0.7*Vcc)
Input Fall Time	tF		300	ns	From (VIH,MIN=0.7*Vcc) to (VIL,MAX=0.3*Vcc)
STOP Setup Time	tSU.STO	0.6		μs	

11. Management Interface Timing

Parameter	Symbol	Fast Mode (400 kHz)	Fast Mode (400 kHz)	Unit	Conditions
Parameter	Symbol	Min	Max	Unit	Conditions
STOP Hold Time	tHD.STO	0.6		us	
Aborted sequence bus release	Deselect _Abort		2	ms	Delay from a host de-asserting ModSelL (at any point in a bus sequence) to the QSFP112 module releasing SCL and SDA
ModSelL Setup Time1	tSU.ModSelL	2		ms	ModSelL Setup Time is the setup time on the select line before the start of a host initiated serial bus sequence.
ModSelL Hold Time1	tHD.ModSelL	2		ms	ModSelL Hold Time is the delay from completion of a serial bus sequence to changes of module select status.
Serial Interface Clock Holdoff “Clock Stretching”	T_clock_hold		500	us	Time the QSFP112 module may hold the SCL line low before continuing with a read or write operation.
Complete Single or Sequential Write to non- volatile registers	tWR		80	ms	Time to complete a Single or Sequential Write to non-volatile registers.

Parameter	Symbol	Fast Mode (400 kHz)	Fast Mode (400 kHz)	Unit	Conditions
Accept a single or sequential write to volatile memory.	tNACK		10	ms	Time to complete a Single or Sequential Write to volatile registers.
Time to complete a memory bank/page	tBPC		10	ms	Time to complete a memory bank and/or page change.
Endurance (Write Cycles)		50k		cycles	Module Case Temperature= 70 °C

12. Timing Characteristics

Parameter	Symbol	Min	Max	Unit	Conditions
MgmtInitDuration	Max MgmtInit Duration		2000	ms	Time from power on1, hot plug or rising edge of reset until until the high to low SDA transition of the Start condition for the first acknowledged TWI transaction.
ResetL Assert Time	t_reset_init	10		μs	Minimum pulse time on the ResetL signal to initiate a module reset.
Int/RxLOS Mode Change	t_IntL/RxLOSL		100	ms	Time to change between IntL and RxLOSL modes of the dual- mode signal IntL/RxLOSL.
LPMode/TxDis mode change time	t_LPMode/TxDis		100	ms	Time to change between LPMode and TxDis modes of LPMode/TxDis.
IntL Assert Time	ton_IntL		200	ms	Time from occurrence of condition triggering IntL until Vout:IntL=Vol.
IntL Deassert Time	toff_IntL		500	μs	Time from clear on read2 operation of associated flag until Vout:IntL=Voh. This includes deassert times for Rx LOS, Tx Fault and other flag bits.
Parameter	Symbol	Min	Max	Unit	Conditions
Rx LOS Assert Time	ton_los		100	ms	Time from Rx LOS condition present to Rx LOS bit set (value = 1b) and IntL asserted.
Rx LOS Assert Time (optional fast mode)	ton_losf		1	ms	Time from Rx LOS state to Rx LOS bit set (value = 1b) and IntL asserted3.

Parameter	Symbol	Min	Max	Unit	Conditions
RxLOS Deassert Time (optional fast mode)	toff_f_LOS		3	ms	Optional fast mode is advertised via the CMIS [5]. Time from optical signal above the LOS deassert threshold to when the module releases the RxLOSL signal to high.
TX Disable Assert Time	ton_TxDis		100	ms	Time from Tx Disable bit set to 1 until optical output falls below 10% of nominal.
TX Disable Assert Time (optional fast mode)	ton_f_TxDis		3	ms	Optional fast mode is advertised via CMIS [5]. Time from TxDis signal high to the optical output reaching the disabled level.
TX Disable Deassert Time	toff_TxDis		400	ms	Time from Tx Disable bit cleared to 1 until optical output rises above 90% of nominal4.
Tx Fault Assert Time	ton_Txfault		200	ms	Time from Tx Fault state to Tx Fault bit set (value=1b) and IntLasserted.
Flag Assert Time	ton_flag		200	ms	Time from occurrence of condition triggering flag to associated flag bit set (value=1b) and IntL asserted.
Mask Assert Time	ton_mask		100	ms	Time from mask bit set (value=1b)5 until associated IntL assertion is inhibited.
Mask Deassert Time	toff_mask		100	ms	Time from mask bit cleared (value=0b)5 until associated IntL operation resumes.

13. Timing Characteristics

Parameter	Symbol	Max	Unit	Conditions
Rx Squelch Assert Time	ton_Rxsq	15	ms	Time from loss of Rx input signal until the squelched output condition is reached.
Tx Squelch Assert Time	ton_Txsq	400	ms	Time from loss of Tx input signal until the squelched output condition is reached,
Tx Squelch De- assert Time	toff_Txsq	1.5	s	Tx squelch deassert is system and implementation dependent.
Tx Disable Assert Time	ton_txdis	100	ms	Time from the stop condition of the Tx Disable write sequence1 until optical output falls below 10% of nominal.

Parameter	Symbol	Max	Unit	Conditions
Tx Disable Assert Time (optional fast mode)	ton_txdisf	3	ms	Time from Tx Disable bit set (value = 1b)1 until optical output falls below 10% of nominal and see notes 2 and 3.
Tx Disable De- assert Time	toff_txdis	400	ms	Time from Tx Disable bit cleared (value = 0b)1 until optical output rises above 90% of nominal and see note 2.
Tx Disable De- assert Time (optional fast mode)	toff_txdisf	10	ms	Time from Tx Disable bit cleared (value = 0b)1 until optical output rises above 90% of nominal, see note 3.
Rx Output Disable Assert Time	ton_rxdis	100	ms	Time from Rx Output Disable bit set (value = 1b)1 until Rx output falls below 10% of nominal
Rx Output Disable De-assert Time	toff_rxdis	100	ms	Time from Rx Output Disable bit cleared (value = 0b)1 until Rx output rises above 90% of nominal.
Squelch Disable Assert Time	ton_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit set (value = 0b)1 until squelch functionality is disabled.
Squelch Disable De-assert Time	toff_sqdis	100	ms	This applies to Rx and Tx Squelch and is the time from bit cleared (value = 0b)1 until squelch functionality is enabled.

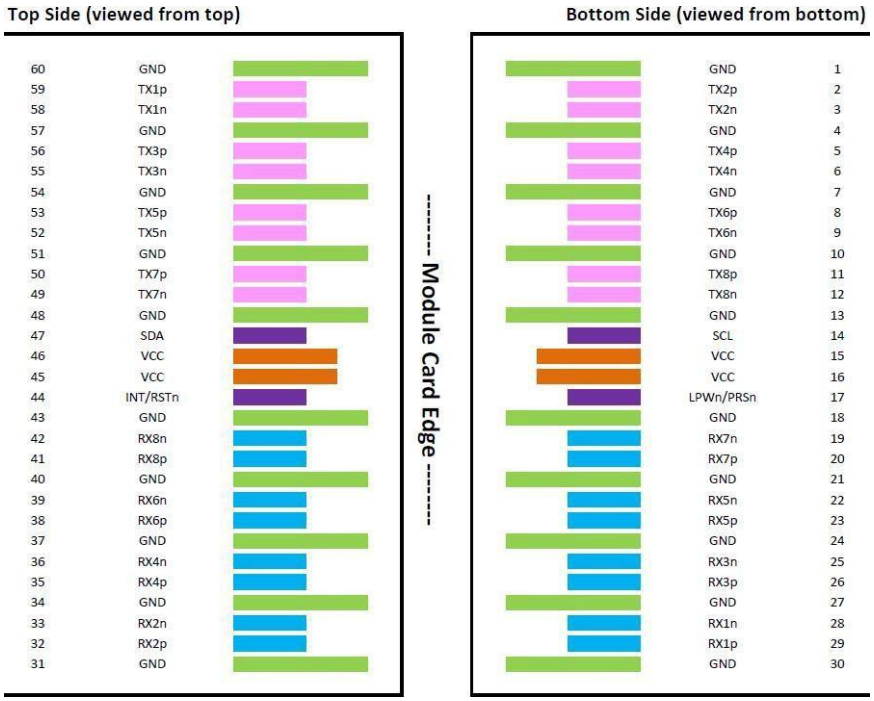
14. Additional Specifications

Code Value	Bit Pattern	Host Electrical Interface	Media Interface
0	00000000b	100GAUI-1-S C2M	100GBASE-SR1
1	00000001b	200GAUI-4	200GBASE-SR4
2	00000010b	100GAUI-4	100GBASE-SR4
3	00000011b	400GAUI-4-S C2M	400GBASE-SR4
4	00000100b	200GAUI-2-S C2M	200GBASE-SR2

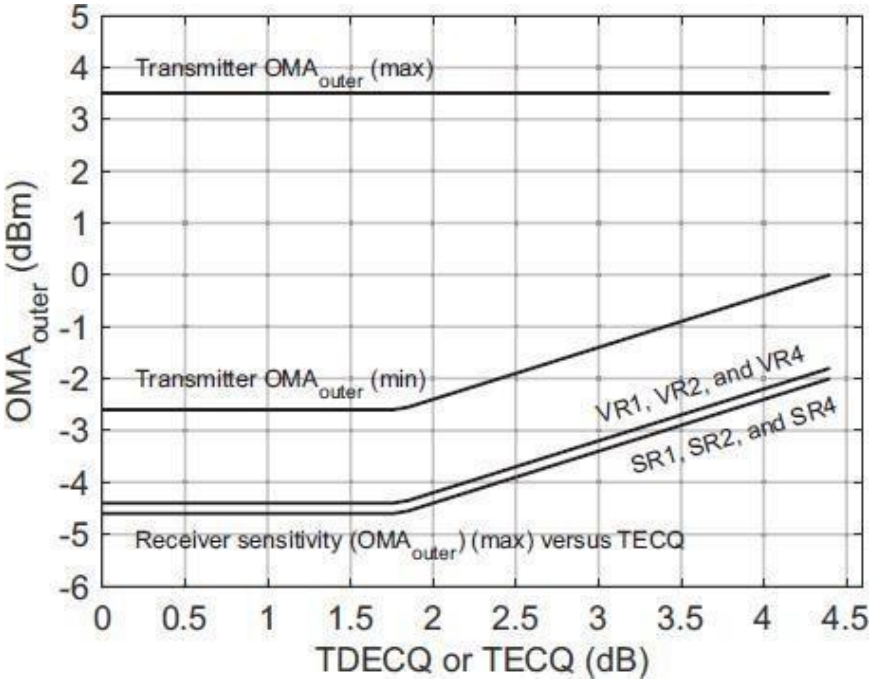
15. Revision History

Version	Initiated	Reviewed	Revision	Release Date
A0	Lynn	Luke	New Release	2023-3-31

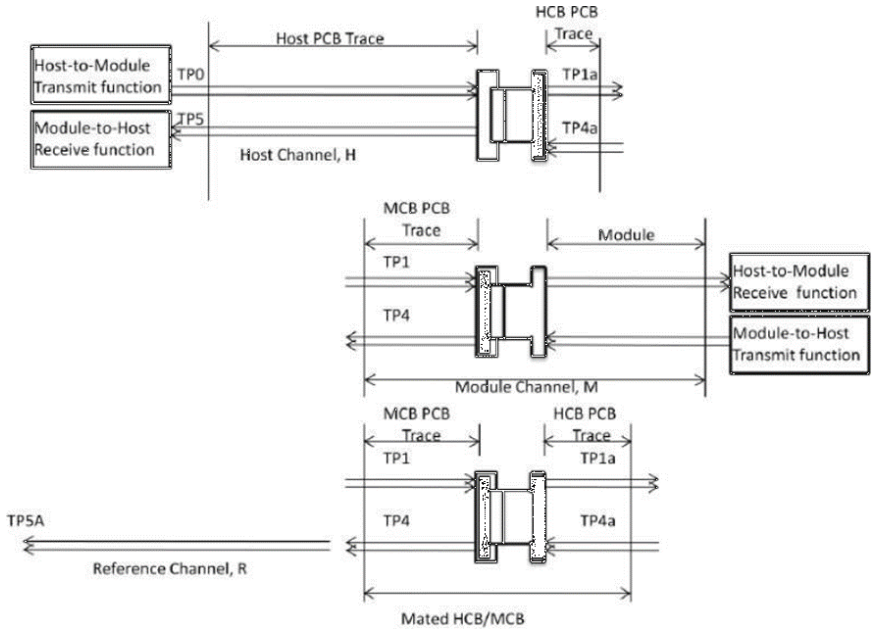
16. Pin Assignment



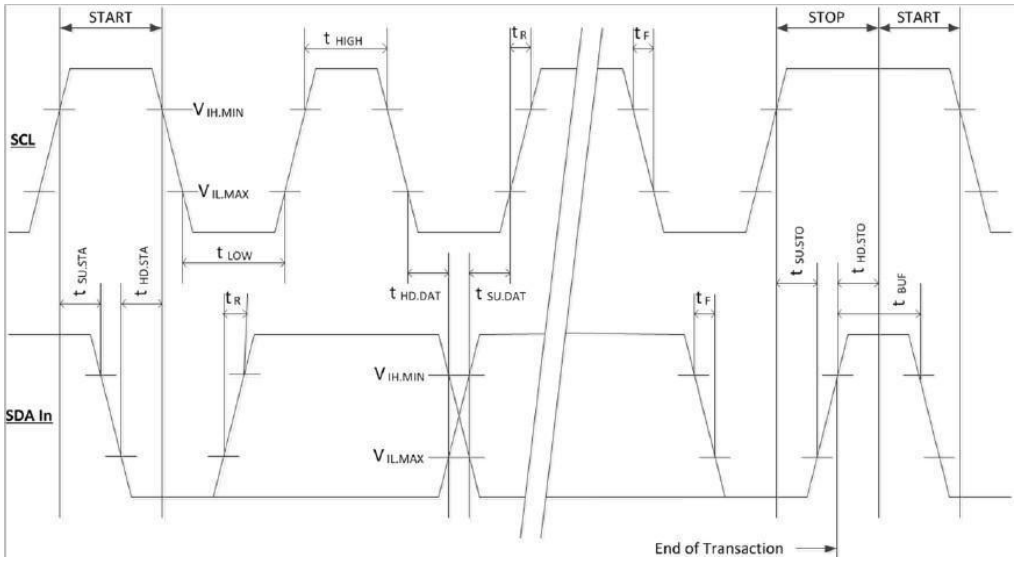
17. Transmitter OMAouter and Receiver Sensitivity versus TDECQ and TECQ



18. High-Speed Electrical Interface Test Points



19. I2C Bus Timing



20. Module Power Classes and CMIS Register Values

Power Class	Max Power (W)	CMIS Register
1	1.5	Direct readout of Page 00h Byte 200[000xxxxx]
2	3.5	Direct readout of Page 00h Byte 200[001xxxxx]
3	7.0	Direct readout of Page 00h Byte 200[010xxxxx]
4	8.0	Direct readout of Page 00h Byte 200[011xxxxx]
5	10	Direct readout of Page 00h Byte 200[100xxxxx]
6	12	Direct readout of Page 00h Byte 200[101xxxxx]
7	14	Direct readout of Page 00h Byte 200[110xxxxx]
8 [1]	>14	Direct readout of Page 00h Byte 200[111xxxxx]
Note: 1. When a module reports power class 8 the host must read CMIS Page 00h Byte 201 to determine module power dissipation. Please see CMIS Byte 201 register definition for more information.		

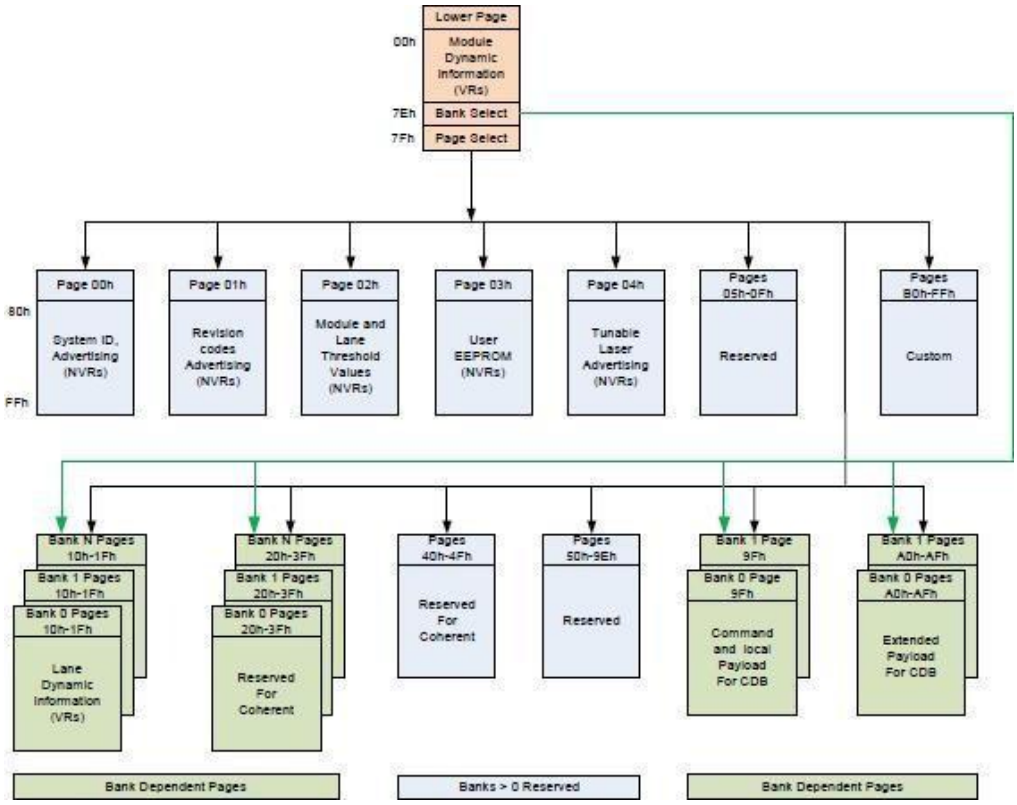
21. Power Supply Requirements

Parameter	Symbol	Minimum	Nominal	Maximum	Units
Module power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Module	3.135	3.300	3.465	V
Host power supply voltage including ripple, droop and noise below 100 kHz	Vcc_Host	3.201	3.300	3.465	V
Voltage drop across mated connector (Vcc_Host minus Vcc_Module)	Vcc_drop			66	mV
Total current for Vcc pins (1)	Icc_module			10.0	A
Host RMS noise output 10 Hz-10 MHz	e_{N_Host}			25	mV
Module RMS noise output 10 Hz - 10 MHz	e_{N_Mod}			15	mV
Module inrush - instantaneous peak duration	T_ip			50	µs
Module inrush - initialization time	T_init			500	ms
Inrush and Discharge Current (2)	I_didt			100	mA/µs
High power mode to Low power mode transition time from assertion of M_LPWn or M_RSTn or ForceLowPwr	T_hplp			200	µs

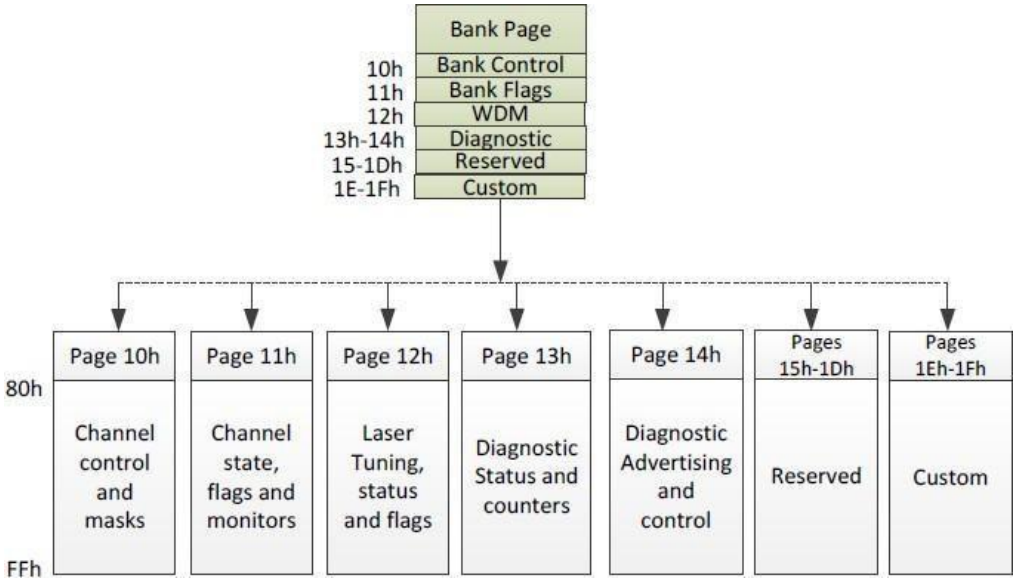
(1) Utilization of the maximum OSFP power rating requires thermal design and validation at the system level to ensure the maximum connector temperature is not exceeded. A recommended design practice is to heatsink the host board power pin pads with multiple vias to a thick copper power plane for conductive cooling.

(2) The specified Inrush and Discharge Current (I_didt) limit shall not be exceeded for all power transient events. This includes hot-plug, hot-unplug, power-up, power-down, initialization, low-power to high-power and high-power to low-power.

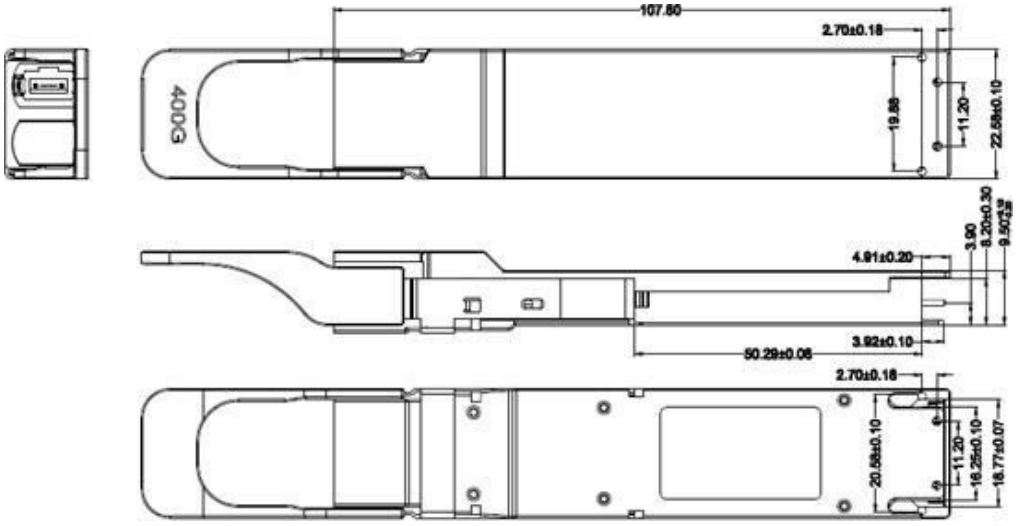
22. CMIS Memory Map



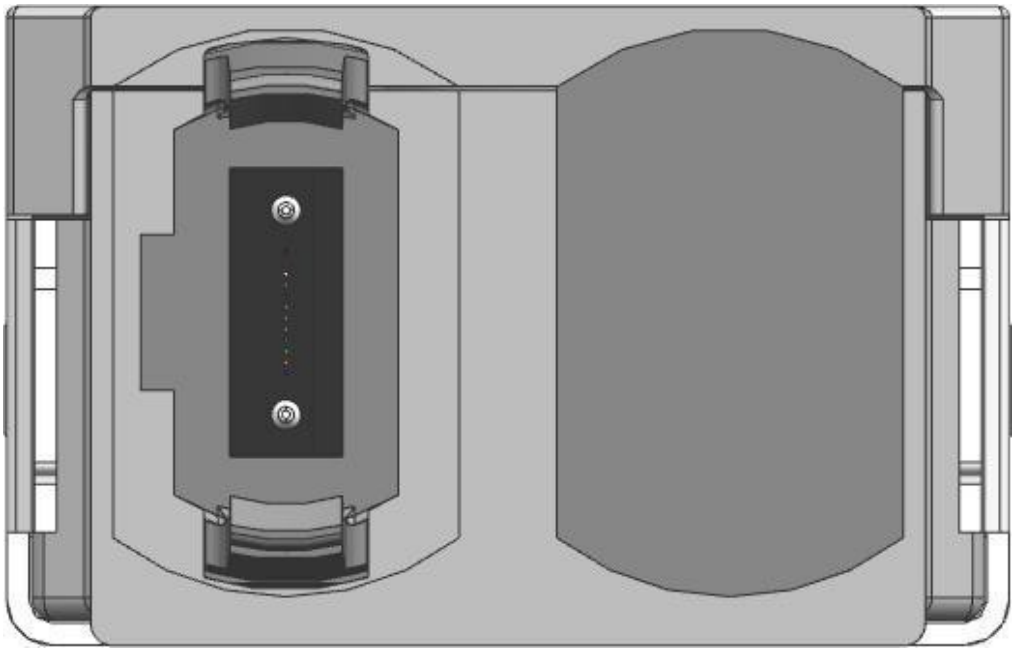
23. CMIS Banked Memory Map



24. Mechanical Specifications



25. Mechanical Specifications



26. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek