WTRQP360

400G QSFP Transceiver SMF 40km LC

Part Number WTRQP360	Data Rate 425Gb/s	Temperature 0~70C



1. Product Overview

Features

- Supports 400GBASE-ER4
- Lane bit rate 106.25Gb/s with PAM4
- Up to 40km transmission on SMF
- Nano-LAN WDM EML laser and SOA+PIN receiver
- 400GAUI-8 Electrical interface with 8 Lanes 53.125 Gb/s PAM4 high-speed signal
- I2C interface with integrated Digital Diagnostic monitoring
- QSFP-DD MSA package with duplex LC connector
- Single +3.3V power supply
- Maximum power consumption 14W
- Operating case temperature: 0 to +70 °C
- Complies with EU Directive 2015/863/EU

Applications

2. Ordering Information

Part No.	Bit Rate (Gbps)	Distance	Fiber Type	DDMI	Connector	Temp
WTRQP360	425Gb/s	40km	SMF	Y	LC	0~70C

3. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Storage Temperature	TS	-40	85	°C	
Supply Voltage	Vcc	-0.5	3.6	V	
Operating Relative Humidity 1,2,3	RH	0	85	%	

4. Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Operating Case Temperature	Tc	0	-	70	°C	
Power Supply Voltage	Vcc	3.13	3.3	3.47	V	
Power Dissipation	P	-	-	14	W	

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Pre-FEC Bit Error Ratio	Pre-FEC BER	-	-	2.4x10-4		1
Post-FEC Bit Error Ratio	Post-FEC BER	-	-	1 x 10-12		1
Transmission Distance	TD	-	-	40	km	2

5. Optical Parameters

Transmitter	Transmitter	Transmitter	Transmitter	Transmitter	Transmitter	Transmitter
Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Signaling rate, each lane	BR	53.125 ± 100 ppm	53.125 ± 100 ppm	53.125 ± 100 ppm	GBd	
Modulation format		PAM4	PAM4	PAM4		
Lane wavelengths	L0	1304.06	1304.58	1305.1	nm	
Lane wavelengths	L1	1306.33	1306.85	1307.38	nm	
Lane wavelengths	L2	1308.61	1309.14	1309.66	nm	
Lane wavelengths	L3	1310.9	1311	1311.96	nm	
Total average launch power	PMAX	-	-	10	dBm	
Average launch power, each lane	POUT	1.5	-	7.1	dBm	1.2
Outer OMA, each lane	OMAouter	4	-	7.9	dBm	3
Difference in launch power between lanes		-	-	4	dB	
Transmitter and dispersion eye closure for PAM4	TDECQ	-	-	3.9	dB	
Transmitter eye closure for PAM4 (TECQ), each lane(max)	TECQ	-	-	3.9	dB	
|TDECQ – TECQ|		-	-	2.7	dB	
Average POUT (Laser Turn off)	POFF	-	-	-30	dBm	
Extinction ratio, each lane	ER	5	-	-	dB	
Side-mode suppression ratio	SMSR	30	-	-	dB	
Receiver	Receiver	Receiver	Receiver	Receiver	Receiver	Receiver
Signaling rate, each lane						
Modulation format		PAM4	PAM4	PAM4		
Lane wavelengths	L0	1304.06	1304.58	1305.1	nm	
Lane wavelengths	L1	1306.33	1306.85	1307.38	nm	
Lane wavelengths	L2	1308.61	1309.14	1309.66	nm	

Transmitter	Transmitter	Transmitter	Transmitter	Transmitter	Transmitter	Transmitter
Lane wavelengths	L3	1310.9	1311	1311.96	nm	
Damage threshold, each lane	PDAMAGE	-2.4	-	-	dBm	4
Average receive power, each lane	PRX _LANE	-16.2	-	-3.4	dBm	5
Receive power (OMAouter), each lane	RXOMA	-	-	-2.6	dBm	
Receiver sensitivity (OMAouter), each lane	SENOMA	-	-	-14.5	dBm	6
Los De-assert	LosDA	-	-	-17	dBm	
Los Hystersis	LosH	0.5	-	-	dB	

6. Electrical Characteristics

Transmitter (Module Input)	Transmitter (Module Input)	Transmitter (Module Input)	Transmitter (Module Input)	Transmitter (Module Input)	Transmitter (Module Input)	Transmitter (Module Input)
Parameter	Parameter	Symbol	Min.	Typical	Max.	Unit
Differential Data Input Amplitude	Differential Data Input Amplitude	VIN,P-P	70	-	900	mVpp
Differential Termination Mismatch	Differential Termination Mismatch		-	-	10	%
Tx_Disable	Normal Operation	VIL	-0.3	-	0.8	V
Tx_Disable	Laser Disable	VIH	2.0	-	VCC+0.3	V
Receiver (Module Output)	Receiver (Module Output)	Receiver (Module Output)	Receiver (Module Output)	Receiver (Module Output)	Receiver (Module Output)	Receiver (Module Output)
Parameter	Parameter	Symbol	Min.	Typical	Max.	Unit
Differential Data Output Amplitude	Differential Data Output Amplitude	VOUT,P-P	200	-	900	mVpp
Differential Termination Mismatch（1MHZ）	Differential Termination Mismatch（1MHZ）		-	-	10	%
Rx_LOS	Normal Operation	VOL	-	-	0.4	V
Rx_LOS	Lose Signal	VOH	VCC-0.5	-	VCC+0.3	V

7. Digital Diagnostics

Parameter	Range	Accuracy	Unit	Calibration
Temperature	0 to 70	±3	ºC	Internal
Voltage	0 to VCC	0.1	V	Internal
Tx Bias Current Per Lane	0 to 100	10%	mA	Internal
Tx Output Power Per Lane	1.5 to 7.1	±3	dBm	Internal
Rx Power (Each Lane)	- 16.2 to 3.4	±3	dBm	Internal

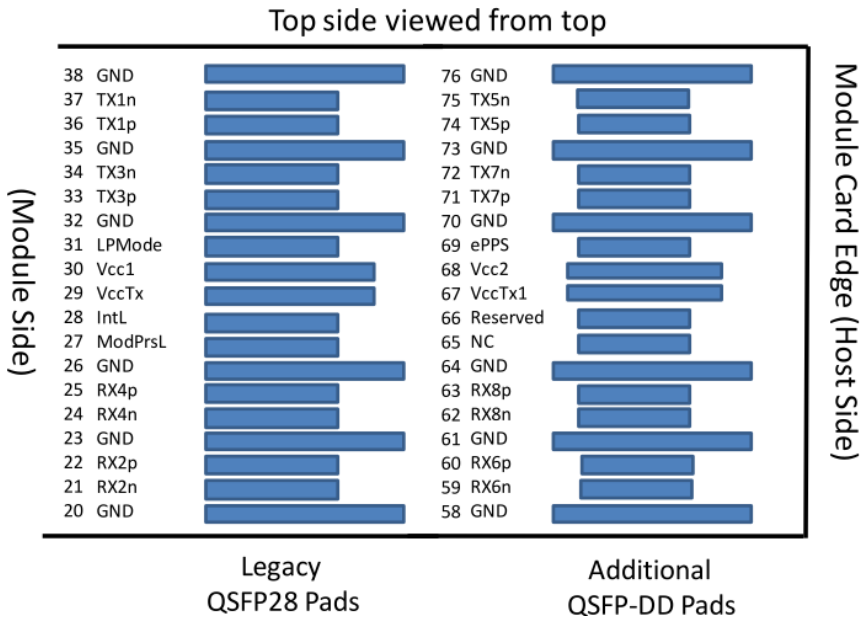
8. Pin Descriptions

PIN	Logic	Symbol	Description	Plug Seq.	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data output	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data output	3B	
7		GND	Ground	1B	1
8	LVTLL-I	ModSelL	Module Select	3B	
9	LVTLL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	3B	
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL/RX_LOS	Interrupt/Rx LOS	3B	

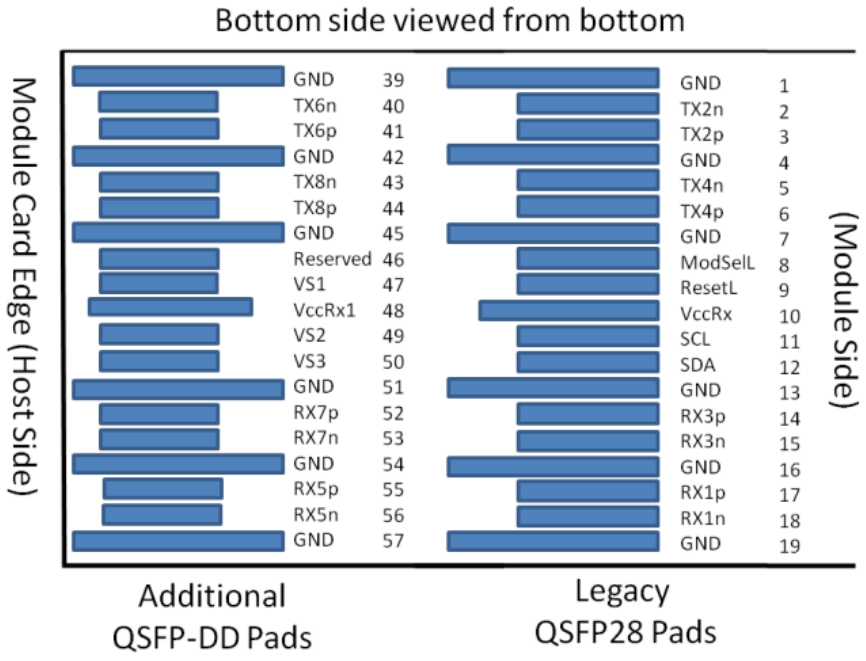
PIN	Logic	Symbol	Description	Plug Seq.	Notes
29		VccTx	+3.3 V Power Supply transmitter	2B	2
30		Vcc1	+3.3 V Power Supply	2B	2
31	LVTTL-I	LPMode/Tx_DIS	Low Power mode/Tx Disable	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	1
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	1
46		Reserved	For future use	3A	3
47		VS1	Module Vendor Specific 1	3A	3
48		VccRx1	3.3V Power Supply	2A	2
49		VS2	Module Vendor Specific 2	3A	3
50		VS3	Module Vendor Specific 3	3A	3
51		GND	Ground	1A	1
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	1
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	1

PIN	Logic	Symbol	Description	Plug Seq.	Notes
58		GND	Ground	1A	1
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	1
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	
63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	1
65		NC	No Connect	3A	3
66		Reserved	For future use	3A	3
67		VccTx1	3.3V Power Supply	2A	2
68		Vcc2	3.3V Power Supply	2A	2
69		Reserved	For future use	3A	3
70		GND	Ground	1A	1
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	1
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	1

9. Technical Figure 1



10. Technical Figure 2



11. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek