WTQD400-DR4

QSFP-DD 400Gb/s DR4 500m Transceiver
/ PRODUCT FEATURES

Part Number
WTQD400-DR4



1. Product Overview

Features

- Aggregation Mode
- 400GBASE-DR4 compliant
- 4x 53.125GBd PAM4
- 400GAUI-8 compliant
- 8x 26.5625 GBd PAM4
- Breakout Mode
- 4x 100GBASE-DR compliant
- 53.125GBd PAM4
- 100GAUI-2 compliant
- 2x 26.5625 GBd PAM4
- QSFP-DD MSA compliant
- MPO-12 connector with 8° angled end-face

Applications

- Data Center 400GE 500 m SMF links
- 400GE to 4x 100GE breakout over 500 m
- Switch/Router interconnections

2. Ordering Information

Part No.	Description
WTQD400-DR4	400G-DR4 QSFP-DD 500m Single Mode Fiber Transceiver, 0 to 70 ºC

3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	Vcc	0	+3.6	V	
Storage Temperature		-40	85	°C	
Optical Receiver Input		-	+5.0	dBm	Average, each lane

4. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR			66	mV	10 Hz –10 MHz
Power Consumption	P_4			8	W	Targer

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Instantaneous peak current	Icc_ip_4			3200	mA	
Sustained peak current	Icc-sp_4			2640.3	mA	
Supply Current	Icc_4			2551.8	mA	Steady state
Case Temperature	TC	0	25	70	°C	

5. Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Channel data rate	fDC	106.25	106.25	106.25	Gb/s	
Signaling rate	fSG	53.125	53.125	53.125	GBd	PAM4
Signal speed variation from nominal	⊿fSG	-100		+100	ppm	
Lane wavelength (range)	C	1304.5		1317.5	nm	
Side-mode suppression ratio	SMSR	30			dB	
Average launch power, each lane		-2.9		4.0	dBm	Note 1
Outer Optical Modulation Amplitude (OMAouter), each lane		-0.8		4.2	dBm	Note 2
Launch power in OMAouter minus TDECQ, each lane		-2.2			dBm	
Transmitter and dispersion eye closure for PAM4, each lane	TDECQ			3.4	dB	
Average Optical Output Power of Off Transmitter, each lane	Poff			-15	dBm	
Extinction Ratio, each lane	ER	3.5			dB	
RIN21.4OMA				-136	dB/Hz	
Optical return loss tolerance				21.4	dB	
Transmitter reflectance				-26	dB	Note 3
Average receive power, each lane		–5.9		4.0	dBm	Note 4
Receive power (OMAouter), each lane				4.2	dBm	
Receiver reflectance				-26	dB	
Receiver sensitivity (OMAouter), each lane		Max (-3.9, SECQ - 5.3), [Figure 3]	Max (-3.9, SECQ - 5.3), [Figure 3]	Max (-3.9, SECQ - 5.3), [Figure 3]		Note 5, 6

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Stressed receiver sensitivity (OMAouter), each lane				-1.9	dBm	Note 5, 7
Conditions of stressed receiver sensitivity test [Note 8]	Conditions of stressed receiver sensitivity test [Note 8]	Conditions of stressed receiver sensitivity test [Note 8]	Conditions of stressed receiver sensitivity test [Note 8]	Conditions of stressed receiver sensitivity test [Note 8]	Conditions of stressed receiver sensitivity test [Note 8]	Conditions of stressed receiver sensitivity test [Note 8]
Stressed eye closure for PAM4 (SECQ), lane under test	SECQ	3.4	3.4	3.4	dB	
OMAouter of each aggressor lane		4.2	4.2	4.2	dBm	

6. Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]	Module output (each lane, at TP4) [Note 1]
Signaling rate per lane (range)	-100ppm	26.5625	+100ppm	GBd	
AC Common-mode output voltage (RMS)	-	-	17.5	mV	
Differential peak-to-peak output voltage	-	-	900	mV	
Near-end ESMW (Eye symmetry mask width)	0.265	-	-	UI	
Near-end Eye height, differential	70			mV	
Far-end ESMW (Eye symmetry mask width)	0.2	-	-	UI	
Far-end Eye height, differential	30	-	-	mV	
Far-end pre-cursor ISI ratio	-4.5	-	2.5	%	
Differential output return loss	Equation (83E-2)	-	-	dB	Note 2
Common to differential mode conversion return loss	Equation (83E-3)	-	-	dB	Note 2
Differential termination mismatch	-	-	10	%	
Transition time (20% to 80%)	9.5	-	-	ps	
DC common mode voltage	-350	-	2850	mV	
Module input (each lane)	Module input (each lane)	Module input (each lane)	Module input (each lane)	Module input (each lane)	Module input (each lane)
Signaling rate per lane (range)	-100ppm	26.5625	+100ppm	GBd	
Differential pk-pk input voltage tolerance	900	-	-	mV	at TP1a

Parameter	Min.	Typ.	Max.	Unit	Remarks
Differential input return loss	Equation (83E-5)	-	-	dB	at TP1, Note 2
Differential to common mode input return loss	Equation (83E-6)	-	-	dB	at TP1, Note 2
Differential termination mismatch	-	-	10	%	at TP1
ESMW (Eye symmetry mask width)	0.22	-	-	UI	at TP1a
Eye width	0.22	-	-	UI	at TP1a
Applied pk-pk sinusoidal jitter	Table 120E–6	Table 120E–6	Table 120E–6	MHz, UI	at TP1a
Eye height	32	-	-	mV	at TP1a
Single-ended input voltage tolerance range	-0.4	-	3.3	V	at TP1a
DC common mode voltage	-350	-	2850	mV	at TP1

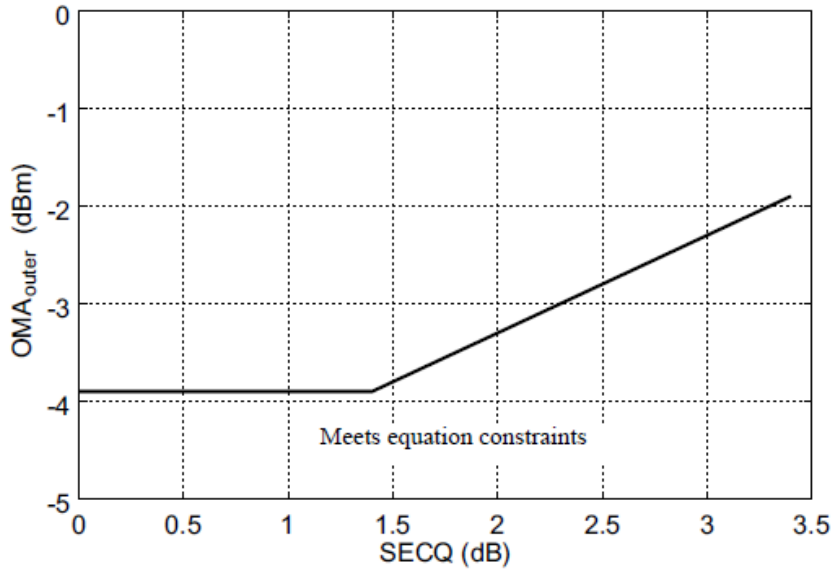
7. Pin Descriptions

Version No.	Date	Description
1.0	May 17, 2023	Specification datasheet

8. Additional Specifications

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Receiver Loss of Signal Indicator Assert Level	RX_LOS	-15	-	-7.9	dBm	Average power
Receiver Loss of Signal Indicator De-assert Level	RX_LOS	-	-	-7.4	dBm	Average power
Hysteresis	RX_LOS	0.5	-	-	dB	

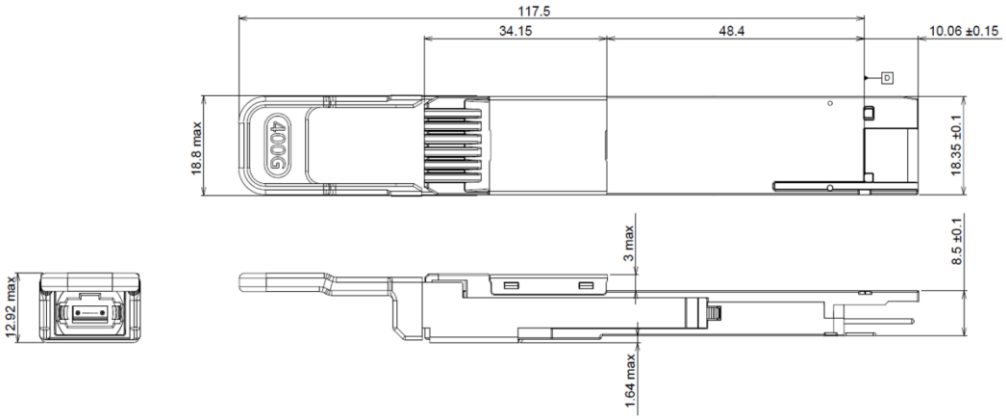
9. Receiver Sensitivity in OMAouter versus SECQ



10. Pin Descriptions

Pad	Logic	Symbol	Description	Plug Sequence[4]	Notes
1		GND	Ground	1B	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	1
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	1
20		GND	Ground	1B	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	1
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	2
30		Vcc1	+3.3V Power supply	2B	2
31	LVTTL-I	LPMode	Low Power mode;	3B	
32		GND	Ground	1B	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	1

11. Mechanical Specifications



12. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek