# WTCFP2-100-ER4C CFP2 ER4 Transceiver

100Gb/s LAN-WDM SMF 40km / Product Overview 3




| Part Number WTCFP2-100-ER4C | Reach 40km SMF | Temperature 0°C~+70°C |
|---|---|---|

## 1. Product Overview

WincoTek 100G CFP2 ER4 optical Transceiver integrates receiver and transmitter path on one module. In the transmit side, four lanes of serial data streams are recovered, retimed, and passed to four laser drivers. The laser drivers control four EMLs (Electric-absorption Modulated Lasers) with center wavelength of 1296 nm, 1300nm, 1305nm and 1309 nm. The optical signals are multiplexed to a single –mode fiber through an industry standard LC connector. In the receive side, the four lanes of optical data streams are optically de-multiplexed by the integrated optical de-multiplexer. Each data stream is recovered by a SOA to amplify，then go to PIN photo-detector and trans-impedance amplifier, retimed. This module features a hot-pluggable electrical interface, low power consumption and MDIO management interface.

The module provides an aggregated signaling rate from 103.125 Gbps to 111.81 Gbps. It is compliant with IEEE 802.3ba 100GBASE-ER4. The MDIO management interface complies with IEEE 802.3ba. The transceiver complies with CFP MSA CFP2 Hardware Specification, CFP MSA Management Interface Specification, and OIF CEI-28G-VSR standards.

### Features

- Compliant with 100GBASE-ER4
- Support line rates from 103.125 Gbps to 111.81 Gbps
- Integrated LAN WDM EML TOSA 、SOA、ROSA for up to 40 km reach over SMF
- Digital Diagnostics Monitoring Interface
- Duplex LC optical receptacle
- No external reference clock
- Single 3.3 V power supply
- Case operating temperature range:0°C to 70°C
- Power dissipation < 9W
- STANDARD
- Compliant to IEEE 802.3ba
- Compliant to CFP MSA Hardware Specification

### Applications

- Data Center &100G Ethernet

## 2. Ordering Information

| Part Number | Data Rate (Gbps) | Laser | Transmission Distance(km) | Temperature (oC) (Operating Case) |
|---|---|---|---|---|
| WTCFP2-100-ER4C | 103.1Gb/s | LWDM | 40km SMF | 0°C~+70°C |

## 3. Absolute Maximum Ratings

| Parameter | Symbol | Min | Typical | Max | Units | Notes |
|---|---|---|---|---|---|---|
| Storage Temperature | Ts | -40 | - | 85 | ºC | |
| Relative Humidity | RH | 5 | - | 95 | % | |
| Power Supply Voltage | VCC | -0.3 | - | 4 | V | |
| Signal Input Voltage | | Vcc-0.3 | - | Vcc+0.3 | V | |
| Receive Input Optical Power (Damage threshold) | Pdmg | | | 5.0 | dBm | |

## 4. Optical Parameters

| Parameter | Symbol | Min | Typ | Max | Unit | NOTE |
|---|---|---|---|---|---|---|
| Transmitter | Transmitter | Transmitter | Transmitter | Transmitter | Transmitter | Transmitter |
| Signaling rate, each lane | | | 25.78125 | | Gbps | |
| Lane wavelength （range） | | 1294.53 | 1295.56 | 1296.59 | nm | |
| Lane wavelength （range） | | 1299.02 | 1300.05 | 1301.09 | nm | |
| Lane wavelength （range） | | 1303.54 | 1304.58 | 1305.63 | nm | |
| Lane wavelength （range） | | 1308.09 | 1309.14 | 1310.19 | nm | |
| Rate tolerance | | -100 | | 100 | ppm | From nominal rate |
| Side-mode suppression ratio | SMSR | 30 | | | dB | |
| Total launch power | | | | 8.9 | dBm | |
| Average launch power, each lane | Pavg | -2.9 | | 2.9 | dBm | |
| Extinction Ratio | ER | 8 | | | dB | |
| Optical modulation amplitude, each lane (OMA) | OMA | 0.1 | | | dBm | |
| Difference in launch power between any two lanes (OMA) | | | | 3.6 | dB | |
| Transmitter and Dispersion Penalty, each lane | TDP | | | 2.5 | dB | |
| Average launch power of OFF transmitter, each lane | | | | -30 | dBm | |
| Transmitter reflectance | | | | -12 | dB | |
| Transmitter eye mask {X1, X2, X3, Y1, Y2, Y3} | | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | {0.25, 0.4, 0.45, 0.25, 0.28, 0.4} | | |
| Receiver | Receiver | Receiver | Receiver | Receiver | Receiver | Receiver |

| Parameter | Symbol | Min | Typ | Max | Unit | NOTE |
|---|---|---|---|---|---|---|
| Signaling rate, each lane | | | 25.78125 | | Gbps | |
| Rate tolerance | | -100 | | 100 | ppm | From normal rate |
| Average receive power, each lane | Pavg | -20.9 | | 4.5 | dBm | |
| Receive power, each lane (OMA) | | | | 4.5 | dBm | |
| Difference in receiver power between any two lanes (OMA) | | | | 4.5 | dB | |
| Receiver Sensitivity (OMA), each lane | Rsen | | | -21.4 | dBm | 1 |
| Stressed Receiver Sensitivity (OMA), each lane | SRS | | | -17.9 | dBm | |
| Stressed receiver sensitivity test conditions | Stressed receiver sensitivity test conditions | Stressed receiver sensitivity test conditions | Stressed receiver sensitivity test conditions | Stressed receiver sensitivity test conditions | Stressed receiver sensitivity test conditions | Stressed receiver sensitivity test conditions |
| Vertical eye closure penalty, each lane | VECP | | 3.5 | | dB | |
| Stressed sys J2 jitter, each lane | J2 | | 0.3 | | UI | 2 |
| Stressed sys J9 jitter, each lane | J9 | | 0.47 | | UI | 2 |
| Receiver reflectance | | | | -26 | dB | |
| LOS Assert | Plos_on | -36 | | | dBm | |
| LOS Deassert | Plos_off | | | -24 | dBm | |
| LOS Hysteresis | | 0.5 | | 4 | dB | |

# 5. Electrical Characteristics

| Parameter | Symbol | Symbol | Min | Typ. | Typ. | Max | Max | Unit | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages | Supply currents and voltages |
| Voltage | Vcc | Vcc | 3.2 | 3.3 | 3.3 | 3.4 | 3.4 | V | V | With Respect to GND |
| Supply current | Icc | Icc | | | | 2.7 | 2.7 | A | A | |
| Power dissipation | Pwr | Pwr | | | | 9.0 | 9.0 | W | W | |
| Power dissipation (low power mode) | Plp | Plp | | | | 2.0 | 2.0 | W | W | |
| Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS | Low speed control and sense signals, 3.3 V LVCMOS |
| Outputs low voltage | Outputs low voltage | VOL | | | | | 0.2 | 0.2 | V | |

| Parameter | Symbol | Symbol | Min | Typ. | Typ. | Max | Max | Unit | Unit | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| Output high voltage | Output high voltage | VOH | Vcc-0.2 | Vcc-0.2 | | | | | V | |
| Input low voltage | Input low voltage | VIL | -0.3 | -0.3 | | | 0.8 | 0.8 | V | |
| Input high voltage | Input high voltage | VIH | 2 | 2 | | | Vcc3+ 0.3 | Vcc3+ 0.3 | V | |
| Input leakage current | Input leakage current | IIN | -10 | -10 | | | 10 | 10 | μA | |
| Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS | Low speed control and sense signals, 1.2 V LVCMOS |
| Outputs low voltage | Outputs low voltage | VOL | -0.3 | -0.3 | | | 0.2 | 0.2 | V | |
| Output high voltage | Output high voltage | VOH | 1.0 | 1.0 | | | 1.5 | 1.5 | V | |
| Output low current | Output low current | IOL | 4 | 4 | | | | | mA | |
| Output high current | Output high current | IOH | | | | | -4 | -4 | mA | |
| Input low voltage | Input low voltage | VIL | -0.3 | -0.3 | | | 0.36 | 0.36 | V | |
| Input high voltage | Input high voltage | VIH | 0.84 | 0.84 | | | 1.5 | 1.5 | V | |
| Input leakage current | Input leakage current | IIN | -100 | -100 | | | 100 | 100 | μA | |
| Input capacitance | Input capacitance | C | | | | | 10 | 10 | pF | |
| MDC clock rate | MDC clock rate | | 0.1 | 0.1 | | | 4 | 4 | MHz | |

# 6. Electrical Characteristics

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Transmitter electrical input from host | Transmitter electrical input from host | Transmitter electrical input from host | Transmitter electrical input from host | Transmitter electrical input from host | Transmitter electrical input from host |
| Differential voltage pk-pk | | 100 | 1200 | mV | |
| Common mode noise (rms) | | | 17.5 | mV | |
| Differential termination mismatch | | | 10 | % | |
| Transition time | | 10 | | ps | 20/80% |
| Common mode voltage | | -0.3 | 2.8 | V | |
| Eye width | EW15 | 0.46 | | UI | At10-15probability |
| Eye height | EH15 | 100 | | mV | At 10-15 probability |
| Receiver electrical output to host | Receiver electrical output to host | Receiver electrical output to host | Receiver electrical output to host | Receiver electrical output to host | Receiver electrical output to host |
| Differential voltage pk-pk | | 100 | 1200 | mV | |

| Parameter | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Common mode noise (rms) | | | 17.5 | mV | |
| Differential termination mismatch | | | 10 | % | |
| Transition time | | 9.5 | | ps | 20/80% |
| Vertical eye closure | VEC | | 6.5 | dB | |
| Eye width | EW15 | 0.57 | | UI | At 10-15 probability |
| Eye height | EH15 | 240 | mV | | At 10-15 probability |

## 7. Pin Descriptions

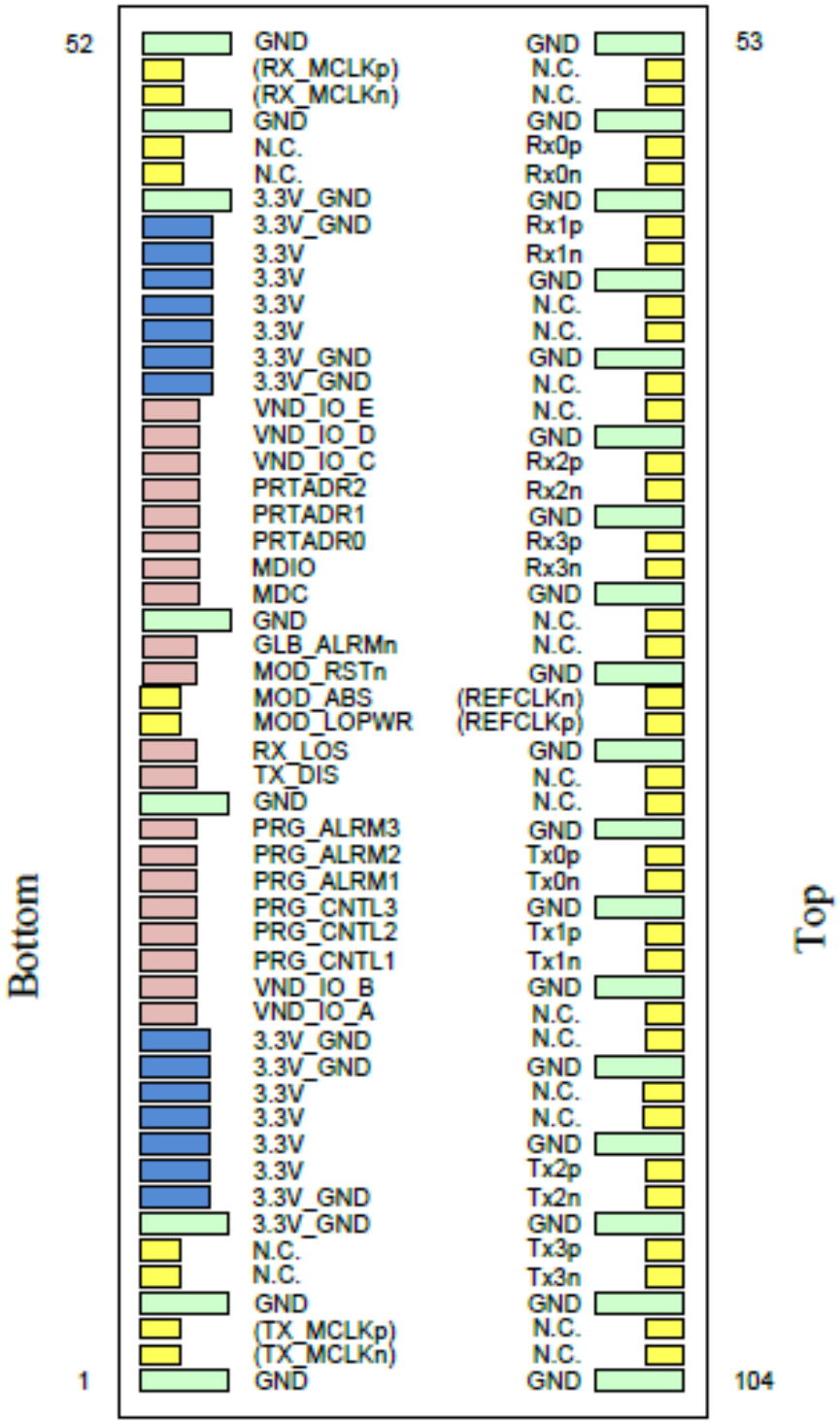
| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 1 | | GND | Module ground |
| 2 | CML | (TX_MCLKn) | No connect |
| 3 | CML | (TX_MCLKp) | No connect |
| 4 | | GND | Module ground |
| 5 | | N.C. | No connect |
| 6 | | N.C. | No connect |
| 7 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 8 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 9 | | 3.3V | 3.3V module supply voltage |
| 10 | | 3.3V | 3.3V module supply voltage |
| 11 | | 3.3V | 3.3V module supply voltage |
| 12 | | 3.3V | 3.3V module supply voltage |
| 13 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 14 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 15 | | VND_IO_A | Module vendor IO A; do not connect |
| 16 | | VND_IO_B | Module vendor IO B; do not connect |
| 17 | LVCMOS1 | PRG_CNTL1 | Programmable control 1; MSA default: TRXIC_RSTn; “0”: reset; “1” or NC: not used |
| 18 | LVCMOS1 | PRG_CNTL2 | Programmable control 2; MSA default: Hardware interlock LSB; Default “0”: ≤ 9 W |
| 19 | LVCMOS1 | PRG_CNTL3 | Programmable control 3: MSA default: Hardware interlock MSB; Default “1”: ≤ 9 W |
| 20 | LVCMOS | PRG_ALRM1 | Programmable alarm 1; MSA default: HIPWR_ON; “1”: module power up completed, “0”: module not high powered up |

| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 21 | LVCMOS | PRG_ALRM2 | Programmable alarm 2; MSA default: MOD_READY, “1”: Ready, “0”: not Ready |
| 22 | LVCMOS | PRG_ALRM3 | Programmable alarm 3; MSA default:: MOD_FAULT, “1”: Fault, “0”: no Fault |
| 23 | | GND | Module ground |
| 24 | LVCMOS1 | TX_DIS | Transmitter disable for all lanes; “1” or NC: transmitter disabled; “0”: transmitter enabled |
| 25 | LVCMOS | RX_LOS | Receiver loss of optical signal; “1”: low optical signal, “0”: normal condition |
| 26 | LVCMOS1 | MOD_LOPWR | Module low power mode; “1” or NC: module in low power mode, “0”: power on enabled |
| 27 | GND | MOD_ABS | Module absent; “1” or NC: module absent; “0”: module present. Pull up resistor on host. |
| 28 | LVCMOS2 | MOD_RSTn | Module reset; “0”: reset the module; “1” or NC: module enabled |
| 29 | LVCMOS | GLB_ALRMn | Global alarm; “0”: alarm in any MDIO alarm register; “1”: no alarm condition. Pull up resistor on host. |
| 30 | | GND | Module ground |
| 31 | 1.2V CMOS | MDC | Management interface clock input |
| 32 | 1.2V CMOS | MDIO | Management interface bi-directional data |
| 33 | 1.2V CMOS | PRTADR0 | MDIO physical port address bit 0 |
| 34 | 1.2V CMOS | PRTADR1 | MDIO physical port address bit 1 |
| 35 | 1.2V CMOS | PRTADR2 | MDIO physical port address bit 2 |
| 36 | | VND_IO_C | Module vendor IO C; do not connect |
| 37 | | VND_IO_D | Module vendor IO D; do not connect |
| 38 | | VND_IO_E | Module vendor IO E; do not connect |
| 39 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 40 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 41 | | 3.3V | 3.3V module supply voltage |
| 42 | | 3.3V | 3.3V module supply voltage |
| 43 | | 3.3V | 3.3V module supply voltage |
| 44 | | 3.3V | 3.3V module supply voltage |
| 45 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 46 | | 3.3V_GND | 3.3V ground; tied with module ground |
| 47 | | N.C. | No connect |

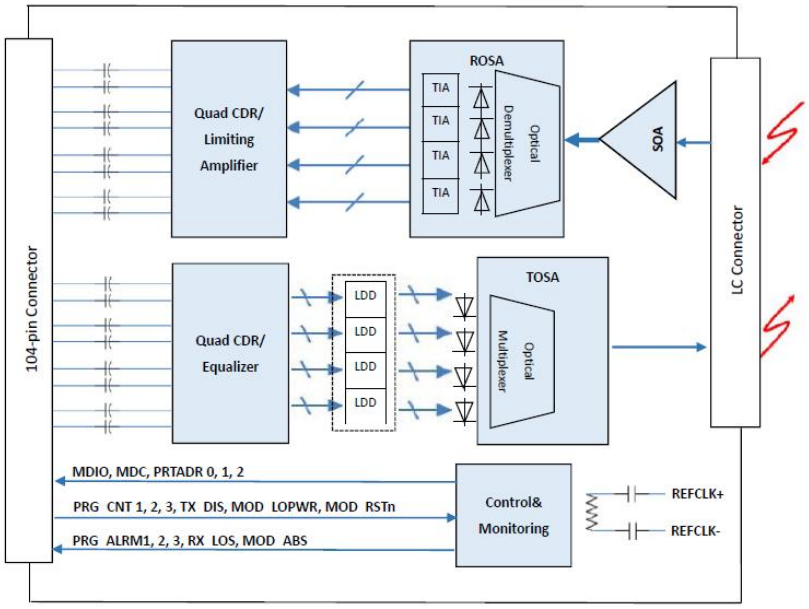
| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 48 | | N.C. | No connect |
| 49 | | GND | Module ground |
| 50 | CML | (RX_MCLKn) | No connect |
| 51 | CML | (RX_MCLKp) | No connect |
| 52 | | GND | Module ground |
| 53 | | GND | Module ground |
| 54 | | N.C. | No connect |
| 55 | | N.C. | No connect |
| 56 | | GND | Module ground |
| 57 | | RX0P | 25 Gbps receiver data; Lane 0 |
| 58 | | RX0n | 25 Gbps receiver data bar; Lane 0 |
| 59 | | GND | Module ground |
| 60 | | RX1p | 25 Gbps receiver data; Lane 1 |
| 61 | | RX1n | 25 Gbps receiver data bar; Lane 1 |
| 62 | | GND | Module ground |
| 63 | | N.C. | No connect |
| 64 | | N.C. | No connect |
| 65 | | GND | Module ground |
| 66 | | N.C. | No connect |
| 67 | | N.C. | No connect |
| 68 | | GND | Module ground |
| 69 | | RX2p | 25 Gbps receiver data; Lane 2 |
| 70 | | RX2n | 25 Gbps receiver data bar; Lane 2 |
| 71 | | GND | Module ground |
| 72 | | RX3p | 25 Gbps receiver data; Lane 3 |
| 73 | | RX3n | 25 Gbps receiver data bar; Lane 3 |
| 74 | | GND | Module ground |
| 75 | | N.C. | No connect |
| 76 | | N.C. | No connect |
| 77 | | GND | Module ground |
| 78 | CML | (REFCLKp) | Module reference clock. No connect. |
| 79 | CML | (REFCLKn) | Module reference clock. No connect. |
| 80 | | GND | Module ground |
| 81 | | N.C. | No connect |
| 82 | | N.C. | No connect |
| 83 | | GND | Module ground |

| Pin no. | Name | Logic | Description |
|---|---|---|---|
| 84 | | TX0p | 25 Gbps transmitter data; Lane 0 |
| 85 | | TX0n | 25 Gbps transmitter data bar; Lane 0 |
| 86 | | GND | Module ground |
| 87 | | TX1p | 25 Gbps transmitter data; Lane 1 |
| 88 | | TX1n | 25 Gbps transmitter data bar; Lane 1 |
| 89 | | GND | Module ground |
| 90 | | N.C. | No connect |
| 91 | | N.C. | No connect |
| 92 | | GND | Module ground |
| 93 | | N.C. | No connect |
| 94 | | N.C. | No connect |
| 95 | | GND | Module ground |
| 96 | | TX2p | 25 Gbps transmitter data; Lane 2 |
| 97 | | TX2n | 25 Gbps transmitter data bar; Lane 2 |
| 98 | | GND | Module ground |
| 99 | | TX3p | 25 Gbps transmitter data; Lane 3 |
| 100 | | TX3n | 25 Gbps transmitter data bar; Lane 3 |
| 101 | | GND | Module ground |
| 102 | | N.C. | No connect |
| 103 | | N.C. | No connect |
| 104 | | GND | Module ground |

## 8. Technical Figure 1



## 9. Technical Figure 2




## 10. Revision History

| Version | Date | Description | Prepared by |
|---|---|---|---|
| V6 | 2025 | Unified WincoTek datasheet format | WincoTek |
| V6.1 | 2026-10-23 | Engineering and format review | WincoTek |