WTQP100-DR1

QSFP28 100Gb/s DR 500m Transceiver /
PRODUCT FEATURES

Part Number
WTQP100-DR1



1. Product Overview

Features

- IEEE 100GBASE-DR compliant
- 100GE Single Protocol (103.125 Gb/s)
- CAUI-4 compliant - 4x 25.78125 Gb/s
- 100GAUI-4 compliant – 4x 26.5625 Gb/s
- RS-FEC(544,514) FEC coder/decoder function
- < 3.5 W MAX
- 0 to 70ºC
- Single cooled 100Gb/s 1310nm EML
- Single PIN PD + low-power TIA
- SFF-8636 management interface

Applications

- Data Center 100G 500m SMF links
- Switch/Router interconnections

2. Ordering Information

Part No.	Description
WTQP100-DR1	100GBASE-DR QSFP28 500m Single Mode Fiber Transceiver, 0 to 70 ºC

3. Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	Remarks
Supply Voltage	Vcc	0	+3.6	V	+3.3 V
Storage Temperature		-40	85	°C	
Optical Receiver Input		-	+5.0	dBm	Average

4. Absolute Maximum Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply Voltage	Vcc	3.135	3.3	3.465	V	
Supply Voltage Noise Tolerance	PSNR	-	-	66	mV	10 Hz –10 MHz
Power Consumption		-	-	3.5	W	Target
Supply Current		--	-	1010.1	mA	Steady state
Case Temperature	TC	0	25	70	°C	

5. Absolute Maximum Ratings

Description	Value	Unit	Notes
Transmitter	Transmitter	Transmitter	Transmitter
PAM4 Signaling rate (range)	53.125 ± 100 ppm	GBd	
Lane wavelengths (range)	1304.5- 1317.5	nm	
Side-mode suppression ratio (SMSR), (min)	30	dB	
Average launch power (max)	4	dBm	
Average launch power (min)	-2.9	dBm	1
Outer Optical Modulation Amplitude (OMAouter) (max)	4.2	dBm	
Outer Optical Modulation Amplitude (OMAouter) (min)	-0.8	dBm	2
Launch power in OMAouter minus TDECQ (min) ER≥5dB2	-2.2	dBm	
Launch power in OMAouter minus TDECQ (min) ER<5dB2	-1.9	dBm	
Transmitter and dispersion penalty Eye Closure for PAM4 (TDECQ), (max)	3.4	dB	
TDECQ – 10*log10(Ceq) (max)	3.4	dB	4
Average launch power of OFF transmitter (max)	-15	dBm	
Extinction ratio (min)	3.5	dB	
Optical return loss tolerance (max)	15.5	dB	
Transmitter reflectance (max)	-26	dB	3
Transmitter transition time (max)	17	ps	
RIN15.5 OMA (max)	-136	dB/Hz	
Receiver	Receiver	Receiver	Receiver
PAM4 Signaling rate (range)	53.125 ± 100 ppm	GBd	
Lane wavelengths (range)	1304.5 to 1317.5	Nm	
Damage threshold (min)	5	dBm	5
Average receive power (max)	4	dBm	
Average receive power (min)	-5.9	dBm	6
Receive power (OMAouter) (max)	4.2	dBm	
Receiver reflectance (max)	-26	dB	
Receiver sensitivity (OMAouter) (max)	max(-3.9, SECQ - 5.3)	dBm	7
Stressed receiver sensitivity (OMAouter) (max)	-1.9	dBm	8
Conditions of stressed receiver sensitivity test	Conditions of stressed receiver sensitivity test	Conditions of stressed receiver sensitivity test	9

Description	Value	Unit	Notes
Stressed eye closure for PAM4 (SECQ)	3.4	dB	
SECQ – 10*log10(Ceq) (max)	3.4	dB	10

6. Electrical Characteristics

Parameter	Min.	Typ.	Max.	Unit	Remarks
Transmitter (each lane)	Transmitter (each lane)	Transmitter (each lane)	Transmitter (each lane)	Transmitter (each lane)	Transmitter (each lane)
Differential pk-pk input voltage tolerance (min)	900	-	-	mV	at TP1a
Differential termination mismatch	-	-	10	%	at TP1
Single-ended input voltage tolerance range	-0.4 to 3.3	-	-	V	at TP1a
DC common mode voltage	-350	-	2850	mV	at TP1
Receiver (each lane, at TP4)	Receiver (each lane, at TP4)	Receiver (each lane, at TP4)	Receiver (each lane, at TP4)	Receiver (each lane, at TP4)	Receiver (each lane, at TP4)
AC Common-mode output voltage (RMS)	-	-	17.5	mV	
Differential output voltage	-	-	900	mV	
Eye width	0.57	-	-	UI	
Eye height, differential	228	-	-	mV	
Vertical eye closure	-	-	5.5	dB	
Differential termination mismatch	-	-	10	%	
Transition time (20% to 80%)	12	-	-	ps	
DC common mode voltage	-350	-	2850	mV	

7. Pin Descriptions

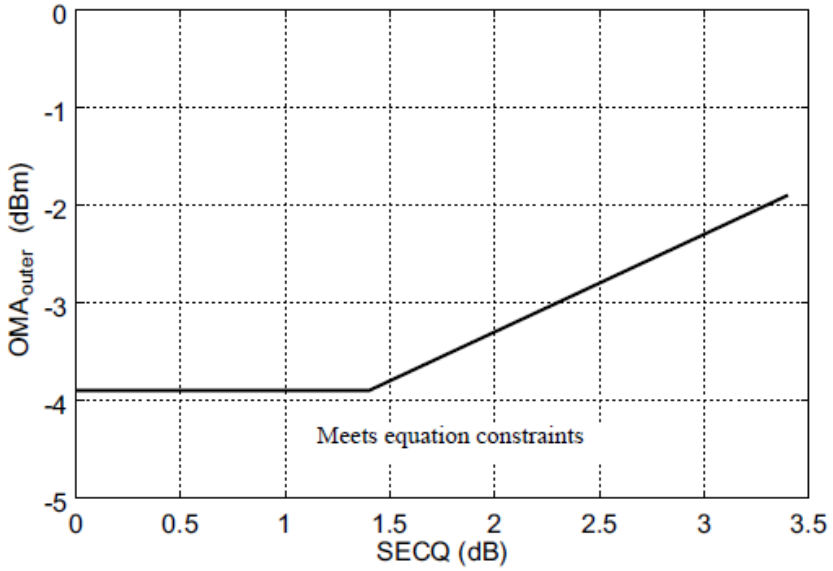
Version No.	Date	Description
1.0	May 17, 2023	Preliminary datasheet

8. Additional Specifications

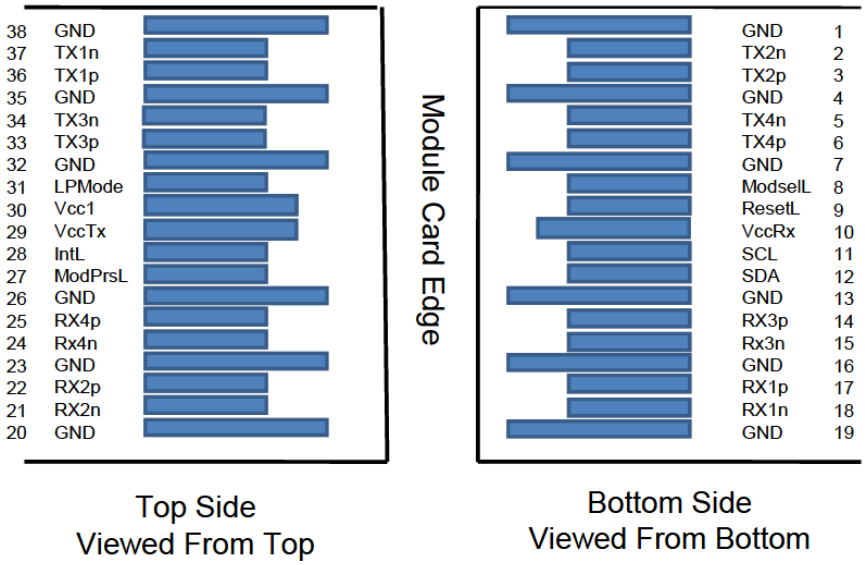
Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Receiver Loss of Signal Indicator Assert Level	RX_LOS	-30	-	-7.5	dBm	Average power

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
Receiver Loss of Signal Indicator De-assert Level	RX_LOS	-	-	-7	dBm	Average power

9. OMAouter Limits versus SECQ



10. Pin Assignment



Top Side
Viewed From Top

Bottom Side
Viewed From Bottom

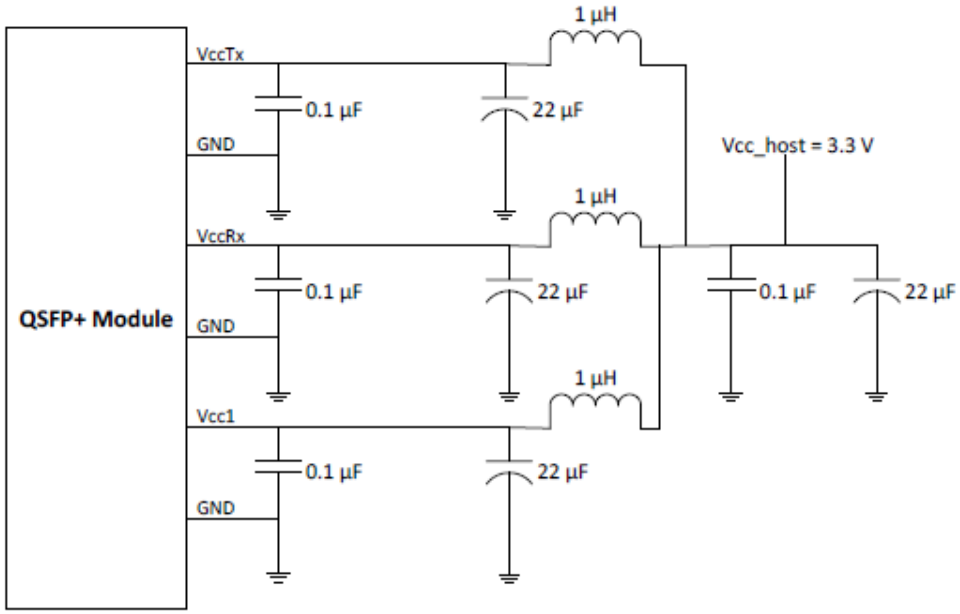
11. Pin Descriptions

Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1	1
2	CML-I	Tx2n	Transmitter Inverted Data Input	3	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3	
4		GND	Ground	1	1
5	CML-I	Tx4n	Transmitter Inverted Data Input	3	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3	
7		GND	Ground	1	1
8	LVTTL-I	ModSelL	Module Select	3	
9	LVTTL-I	ResetL	Module Reset	3	
10		Vcc Rx	+3.3V Power Supply Receiver	2	2
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3	
13		GND	Ground	1	1
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3	
15	CML-O	Rx3n	Receiver Inverted Data Output	3	
16		GND	Ground	1	1
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3	
18	CML-O	Rx1n	Receiver Inverted Data Output	3	
19		GND	Ground	1	1
20		GND	Ground	1	1
21	CML-O	Rx2n	Receiver Inverted Data Output	3	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3	
23		GND	Ground	1	1
24	CML-O	Rx4n	Receiver Inverted Data Output	3	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3	
26		GND	Ground	1	1
27	LVTTL-O	ModPrsL	Module Present	3	
28	LVTTL-O	IntL	Interrupt	3	
29		Vcc Tx	+3.3V Power supply transmitter	2	2
30		Vcc1	+3.3V Power supply	2	2
31	LVTTL-I	LPMode	Low Power Mode	3	
32		GND	Ground	1	1
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3	
35		GND	Ground	1	1
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3	
38		GND	Ground	1	1

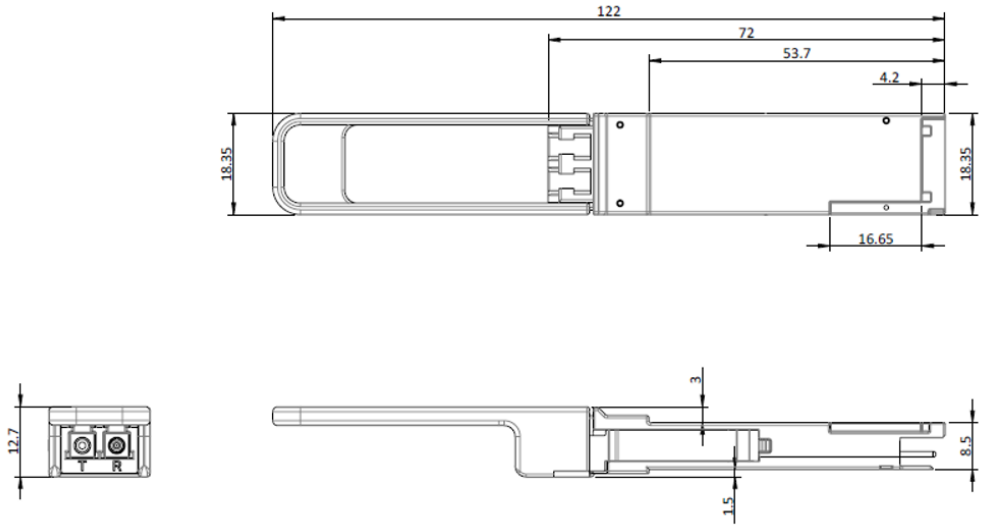
Note 1: GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are referenced to this potential unless otherwise noted. Connect these directly to the host board signal-common ground plane.

Note 2: Vcc Rx, Vcc1 and Vcc Tx shall be applied concurrently. Requirements defined for the host side of the Host Edge Card Connector are listed in Table 5-6. Vcc Rx Vcc1 and Vcc Tx may be internally connected within the module in any combination. The connector pins are each rated for a maximum current of 1000 mA.

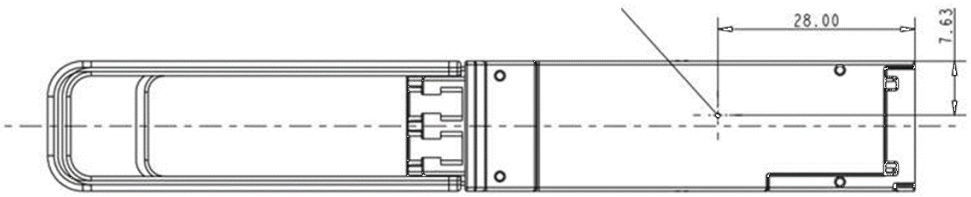
12. Recommended Interface Circuit



13. Mechanical Specifications



14. Mechanical Specifications



15. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek