100G_200G MR CFP2 DCO Product Specification

Introduction / This document describes the product specifications for coherent 100G/200G CFP2 DCO modules based on dual polarization quadrature phase shift keying (DP-QPSK) or dual polarization quadrature amplitude modulation (DP-16QAM) supporting extended C-band, polarization diversity coherent detection and advanced electronic link equalization. The module can accommodate various client signals such as 100 Giga-bit Ethernet (100GbE) and Optical Transport channel Uint-4(OUT4). The module will enable the following system performance and features:



1. Product Overview

Features

- 100G/200G coherent CFP2 DCO product variants.
- 100G DP-QPSK and 200G DP-16QAM operation with oFEC.
- Single-channel tunable operation in the extended C-band.
- Operating case temperature: 0 to 70 °C.

Applications

2. Ordering Information

Product	Description	Note
CT-WTCTS100SMRTA00	Single rate 100Gb/s single channel tunable coherent CFP2 MR with DP-QPSK oFEC, 0 ~ 70℃;	
CT-WTCTS200SMRTA00	Single rate 200Gb/s single channel tunable coherent CFP2 MR with DP-16QAM oFEC, 0 ~ 70℃;	

3. Absolute Maximum Ratings

Item	Parameter	Condition (1)	Min	Max	Unit
1	Storage Temperature Range		-40	85	℃
2	Storage Humidity	Relative, no-Condensing	-	85	%
3	Case Temperature Range		0	+75	℃
4	Power supply		-0.3	3.7	V
5	Input power (Optical)	Peak Power		10	dBm

4. Absolute Maximum Ratings

Item	Parameter	Condition	Symbol	Min	Max	Unit
1	Operating Case Temperature (Top)		Tcase	0	70	℃
2	Relative humidity Range	Non-condensing	RH	-	85	%
3	Operating Input Optical Power of Signal		Psig	-18	+5	dBm
4	Storage Temperature Range			-40	85	℃

5. Recommended Operating Conditions

Item	Parameter	Condition	Min	Typ	Max	Unit
1	3.3V DC Power Supply Voltage		3.2	3.3	3.4	V
2	3.3V DC Power Supply Current				8	A
3	Power Consumption	Low Power			2	W
4	Power Consumption @ DP-16QAM with oFEC for 200G			22	24	W
5	Power Consumption @ DP-QPSK with oFEC for 100G			18	21	W
6	Inrush current	Power class 5 & 6			300	mA/us
7	Turn-off current	Power class 5 & 6	-300			mA/us
8	Power Supply Noise	DC - 1MHz			2	%
9	Power Supply Noise	1 - 10MHz			3	%

6. Recommended Operating Conditions

Pin Number	Name of Pin	Structure	Logic	Description / Connection
Pin Number	Name of Pin	(Input/Output)	Logic	Description / Connection

Pin Number	Name of Pin	Structure	Logic	Description / Connection
1	GND	GND	Ground	
2	OHIO_RDn	O	CML	OHIO output: Differential 100Ω built-in,800-1200mVppd
3	OHIO_RDp	O	CML	OHIO output
4	GND	GND	Ground	
5	OHIO_TDn	I	CML	OHIO input: Differential 100Ω built-in,100-1200mVppd
6	OHIO_TDp	I	CML	OHIO input
7	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
8	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
9	3.3V	PWR	Power	3.3V Module Supply Voltage
10	3.3V	PWR	Power	3.3V Module Supply Voltage
11	3.3V	PWR	Power	3.3V Module Supply Voltage
12	3.3V	PWR	Power	3.3V Module Supply Voltage
13	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
14	3.3V GND	PWR_GND	Ground	3.3V Module Supply Voltage Return Ground, can be separate or tied together with Signal Ground
15	VND_IO_A	I/O	LVCMOS	TXD0 of Uart0 (For FPGA: Module to PC)
16	VND_IO_B	I/O	LVCMOS	RXD0 of Uart0 (For FPGA: PC to Module)
17	PRG_CNTL1	I	LVCMOS w/PUR	Programmable Control 1 set over MDIO, MSA Default: TRXIC_RSTn, TX & RX ICs reset, "0": reset, "1" or NC: enabled or not used
18	PRG_CNTL2	I	LVCMOS w/PUR	Programmable Control 2 set over MDIO, MSA Default: Hardware Interlock LSB, "00": ≤9W, "01": ≤12W, "10": ≤ 15W, "11" or NC: ≤18W or not used

Pin Number	Name of Pin	Structure	Logic	Description / Connection
19	PRG_CNTL3	I	LVCMOS w/PUR	Programmable Control 3 set over MDIO, MSA Default: Hardware Interlock MSB, "00": ≤9W, "01": ≤12W, "10": ≤15W, "11" or NC:≤18W or not used
20	PRG_ALRM1	O	LVCMOS	Programmable Alarm 1; MSA Default “H” = HIPWR_ON
21	PRG_ALRM2	O	LVCMOS	Programmable Alarm 2; MSA Default “H” = MOD_READY
22	PRG_ALRM3	O	LVCMOS	Programmable Alarm 3; MSA Default “H” = MOD_FAULT
23	GND	GND	Ground	
24	TX_DIS	I	LVCMOS w/PUR	Transmitter Disable for all lanes, "1" or NC = transmitter disabled, "0" = transmitter enabled

7. Optical Parameters

Id	Parameter	Typ	Min	Max	Unit	Condition/comments
1	Transmitter Frequency Range	193.7	191.3	196.10	THz	C band 50GHz ITU-T grid. Frequency range over which the specifications hold unless noted otherwise.
2	Channel Spacing	50			GHz	
3	Frequency Stability		-2.5	2.5	GHz	Frequency stability relative to ITU grid.
4	Frequency Offset		-2.5	2.5	GHz	
5	Frequency Fine Tuning Range		-6.0	6.0	GHz	
6	Fine Tuning Resolution	100			MHz	
7	Channel Tuning Speed			80	s	
8	Line Width			500	kHz	FWHM
9	SMSR (Side mode suppression Ratio)	45	40		dB	Measured over +/- 2.5nm range around the target frequency with 0.06nm RBW without modulation.
10	Transmitter output power range	0	-5	+5	dBm	Transmitter output is settable in steps of 0.1 dB at any power level within the specified frequency range
11	Output power stability		-0.5	0.5	dB	Difference over temperature, time, wavelength and aging.

Id	Parameter	Typ	Min	Max	Unit	Condition/comments
12	Output power monitor accuracy		-2	2	dB	Difference between the set value and actual value over aging.
13	Transmitter turn-up time from warm start		-	15	ms	Module is in Ready state. The maximum transmitter turn-up time is counted from de-assert the Tx_disable Pin to full Tx turn-up.
14	Transmitter output disable time		-	3	ms	Tx is in full turn-up state. The maximum transmitter turn-off time is counted from assert Tx_disable pin
15	Transmitter turn-up time from cold start		-	90	s	Module is in Low_Power mode. The maximum Tx turn-up time is counted from de-assert the Low_power pin and Tx_disable pin to full Tx turn-up.
16	Transmitter OSNR		35		dB/0.1nm	OSNR at transmitter output (in-band)
17	Transmitter optical return loss		27	-	dB	
18	Transmitter output power with TX disabled			-40	dBm	
19	Transmitter polarization dependent power			1	dB	Power deference between X and Y polarization

8. Optical Parameters

Pin#	Name	Name	Name	Name	Description
Pin#	4x28G NRZ	8x28G NRZ	2x56G PAM4	4x56G PAM4	Description
104	GND	GND	GND	GND	Ground
103	N.C.	TX4n	N.C.	N.C.	Transmitter lane 4
102	N.C.	TX4p	N.C.	N.C.	Transmitter lane 4
101	GND	GND	GND	GND	Ground
100	TX3n	TX3n	N.C.	TX3n	Transmitter lane 3
99	TX3p	TX3p	N.C.	TX3p	Transmitter lane 3
98	GND	GND	GND	GND	Ground
97	TX2n	TX2n	N.C.	TX2n	Transmitter lane 2
96	TX2p	TX2p	N.C.	TX2p	Transmitter lane 2
95	GND	GND	GND	GND	Ground
94	N.C.	TX5n	N.C.	N.C.	Transmitter lane 5
93	N.C.	TX5p	N.C.	N.C.	Transmitter lane 5
92	GND	GND	GND	GND	Ground
91	N.C.	TX6n	N.C.	N.C.	Transmitter lane 6

Pin#	Name	Name	Name	Name	Description
90	N.C.	TX6p	N.C.	N.C.	Transmitter lane 6
89	GND	GND	GND	GND	Ground
88	TX1n	TX1n	TX1n	TX1n	Transmitter lane 1
87	TX1p	TX1p	TX1p	TX1p	Transmitter lane 1
86	GND	GND	GND	GND	Ground
85	TX0n	TX0n	TX0n	TX0n	Transmitter lane 0
84	TX0p	TX0p	TX0p	TX0p	Transmitter lane 0
83	GND	GND	GND	GND	Ground
82	N.C.	TX7n	N.C.	N.C.	Transmitter lane 7
81	N.C.	TX7p	N.C.	N.C.	Transmitter lane 7
80	GND	GND	GND	GND	Ground
79	(REFCLKn)	(REFCLKn)	(REFCLKn)	(REFCLKn)	N.C
78	(REFCLKp)	(REFCLKp)	(REFCLKp)	(REFCLKp)	N.C
77	GND	GND	GND	GND	Ground
76	N.C.	RX4n	N.C.	N.C.	Receiver lane 4
75	N.C.	RX4p	N.C.	N.C.	Receiver lane 4
74	GND	GND	GND	GND	Ground
73	RX3n	RX3n	N.C.	RX3n	

9. Additional Specifications

Client-Side type	Client I/F mode	Client lane rate (Gb/s)	Note
1*100G	1*CAUI-4	4*25Gbps (NRZ)	For 100G
1*OTU4	1*OTL4.4	4*28Gbps (NRZ)	For 100G
2*100G	2*CAUI-4	8*25Gbps (NRZ)	For 200G
2*OTU4	2*OTL4.4	8*28Gbps (NRZ)	For 200G

10. Additional Specifications

Host Frame	Host Data Bit Rate (Gbps)	Offset(ppm)	Singal
1*100G	1*103.125	100	Ethernet class
1*OTU4	1*111.8099736	20	
2*100G	2*103.125	100	Ethernet class
2*OTU4	2*111.8099736	20	

11. Additional Specifications

Id	Application	Modulation	FEC Type	Lane Baud	Grid	OSNR	Note
1	100G	DP-QPSK	oFEC	31.57G	50G	11.5	
2	200G	DP-16QAM	oFEC	31.57G	50G	19.5	

12. Additional Specifications

Id	Parameter	Typ.	Min	Max	Unit	Condition/comments
1	Receiver Frequency Range	193.7	191.3	196.10	THz	C band 50GHz ITU-T grid.
2	Input power range		-18	0	dBm	Signal power of the channel needed to meet the OSNR tolerance requirement
3	Receiver Sensitivity			-21	dBm	Minimum input power needed to achieve post FEC BER < 10-15 when OSNR > 35dB and internal FEC enabled
4	OSNR Sensitivity @100G DP-QPSK	11.5		12.5	dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
5	OSNR Sensitivity @200G DP-16QAM	19.5		21	dB/0.1nm	At internal FEC threshold (post FEC BER < 10-15), at optimum Input power as specified above.
6	Los assert			-29	dBm	
7	Los de-assert			-26	dBm	
8	Los hysteresis			3	dB	
9	CD Tolerance			40000	ps/nm	With less than 0.5dB OSNR penalty at FEC threshold.
10	DGD tolerance		50		ps	DGD tolerance Under the following conditions: 0.5dB OSNR penalty at FEC threshold;
11	PDL tolerance		3		dB	PDL tolerance under the following conditions: PDL applied before noise loading; Change in SOP is <=50rad/millisecond; With additional 1.5dB OSNR penalty
12	Tolerance to change in SOP		50	-	rad/ms	Tolerance to change in SOP with <0.5dB OSNR penalty at FEC threshold.
13	Input power transient tolerance		-2	2	dB	Optical input power transient tolerance Less than 0.5dB OSNR penalty if the received power is within inout power range and rise/fall times of power change (defined by 20-80%) of 50μs or slower.

Id	Parameter	Typ.	Min	Max	Unit	Condition/comments
14	Input power reading accuracy		-1.5	1.5	dB	The module reports the actual power as received by the module.
15	Optical Return Loss		27		dB	
16	Receiver turn-up time from cold start		-	90	Seconds	Module is in Low_power state and valid Rx input signal is ready. The time from de-assert Low_power pin to full Rx turn-up, given that valid line side signal is ready.
17	RX LOS Assert time			3	ms	Assert Time of Receiver Loss of Signal
18	RX LOS De-assert time			3	ms	De-assert Time of Receiver Loss of Signal

13. Additional Specifications

25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
26	MOD_LOPWR	I	LVCMOS w/PUR	Module Low Power Mode. "1" or NC: module in low power (safe) mode, "0": power-on enabled
27	MOD_ABS	O	GND	Module Absent. "1" or NC: module absent, "0": module present, Pull Up Resistor on Host
28	MOD_RSTn	I	LVCMOS w/PUR	Module Reset. "0" resets the module, "1" or NC = module enabled, Pull Down Resistor in Module
29	GLB_ALRMn	O	LVCMOS	Global Alarm. “0": alarm condition in any MDIO Alarm register, "1": no alarm condition, Open Drain, Pull Up Resistor on Host
30	GND	GND	Ground	
31	MDC	I	1.2V LVCMOS	Management Data Clock (electrical specs as per IEEE Std 802.3- 2012)
32	MDIO	I/O	1.2V LVCMOS	Management Data I/O bi-directional data (electrical specs as per IEEE Std 802.3-2012)
33	PRTADR0	I	1.2V LVCMOS	MDIO Physical Port Address bit 0
34	PRTADR1	I	1.2V LVCMOS	MDIO Physical Port Address bit 1
35	PRTADR2	I	1.2V LVCMOS	MDIO Physical Port Address bit 2

25	RX_LOS	O	LVCMOS	Receiver Loss of Optical Signal, "1": low optical signal, "0": normal condition
36	VND_IO_C	I/O	LVCMOS	TMS/SWDIO (PC to Module or Module to PC)
37	VND_IO_D	I	LVCMOS	TCK/SWDCK (PC to Module)
38	VND_IO_E	I/O	LVCMOS	TXD1 of Uart1 (Module to PC)
39	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
40	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
41	3.3V	PWR	Power	3.3V power supply
42	3.3V	PWR	Power	3.3V power supply
43	3.3V	PWR	Power	3.3V power supply
44	3.3V	PWR	Power	3.3V power supply
45	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
46	3.3V GND	PWR_GND	Ground	Power Ground. Internally connected to logic GND. power supply return path.
47	OHIO_REFCLKn	I	CML	OHIO ref clk input,100MHz, ±100ppm，100-1200mVppd
48	OHIO_REFCLKp	I	CML	OHIO ref clk input,Differential 100Ω built-in
49	GND	GND	Ground	Module Ground. Logic and power return path
50	TX_MCKLn	O	CML	TX lineside monitor clock
51	TX_MCKLn	O	CML	TX lineside monitor clock
52	GND	GND	Ground	Module Ground. Logic and power return path

14. Additional Specifications

72	RX3p	RX3p	N.C.	RX3p	Receiver lane 3
71	GND	GND	GND	GND	Ground
70	RX2n	RX2n	N.C.	RX2n	Receiver lane 2
69	RX2p	RX2p	N.C.	RX2p	Receiver lane 2
68	GND	GND	GND	GND	Ground
67	N.C.	RX5n	N.C.	N.C.	Receiver lane 5
66	N.C.	RX5p	N.C.	N.C.	Receiver lane 5
65	GND	GND	GND	GND	Ground
64	N.C.	RX6n	N.C.	N.C.	Receiver lane 6

72	RX3p	RX3p	N.C.	RX3p	Receiver lane 3
63	N.C.	RX6p	N.C.	N.C.	Receiver lane 6
62	GND	GND	GND	GND	Ground
61	RX1n	RX1n	RX1n	RX1n	Receiver lane 1
60	RX1p	RX1p	RX1p	RX1p	Receiver lane 1
59	GND	GND	GND	GND	Ground
58	RX0n	RX0n	RX0n	RX0n	Receiver lane 0
57	RX0p	RX0p	RX0p	RX0p	Receiver lane 0
56	GND	GND	GND	GND	Ground
55	N.C.	RX7n	N.C.	N.C.	Receiver lane 7
54	N.C.	RX7p	N.C.	N.C.	Receiver lane 7
53	GND	GND	GND	GND	Ground

15. Additional Specifications

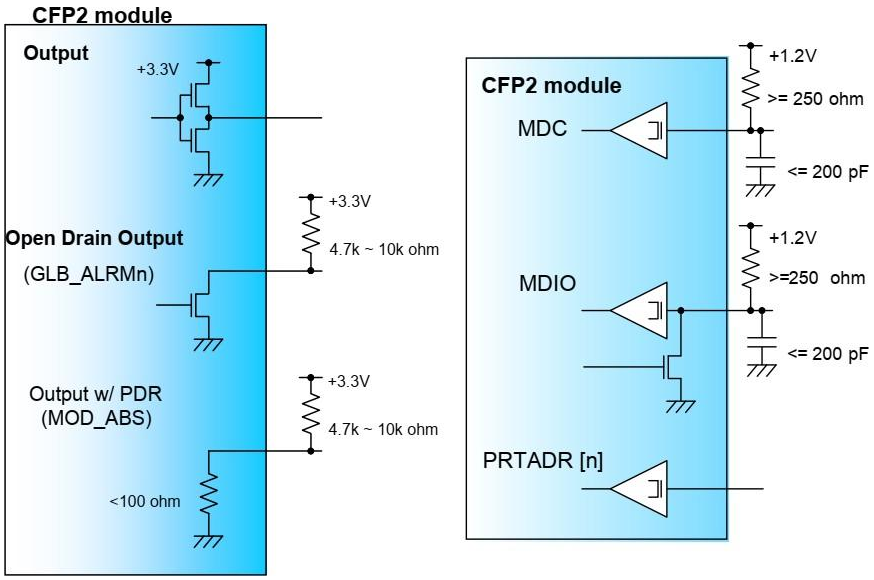
SerDes Lanes	200G	100G
SerDes Lanes	2*CAUI-4 2*OTL4.4 (NRZ)	1*CAUI-4 1*OTL4.4 (NRZ)
SerDes Lanes	Interface - CH[x,y]	Interface - CH[x,y]
Tx7[p,n];Rx7[p,n]	CH2.2	NC
Tx6[p,n];Rx6[p,n]	CH2.2	NC
Tx5[p,n];Rx5[p,n]	CH2.2	NC
Tx4[p,n];Rx4[p,n]	CH2.2	NC
Tx3[p,n];Rx3[p,n]	CH2.1	CH1.1
Tx2[p,n];Rx2[p,n]	CH2.1	CH1.1
Tx1[p,n];Rx1[p,n]	CH2.1	CH1.1
Tx0[p,n];Rx0[p,n]	CH2.1	CH1.1
Note: The CFP2 Host/Client interface naming convention is CH, where, CH=Channel, <x>.<y>: <x> = channel capacity, where [x=1,2] is 1=100G or 2=200G. <y> = channel numeration, where [y=1 …3] is channel numeration. NC – No connected	Note: The CFP2 Host/Client interface naming convention is CH, where, CH=Channel, <x>.<y>: <x> = channel capacity, where [x=1,2] is 1=100G or 2=200G. <y> = channel numeration, where [y=1 …3] is channel numeration. NC – No connected	Note: The CFP2 Host/Client interface naming convention is CH, where, CH=Channel, <x>.<y>: <x> = channel capacity, where [x=1,2] is 1=100G or 2=200G. <y> = channel numeration, where [y=1 …3] is channel numeration. NC – No connected

16. Additional Specifications

Glossary	Info.
ADC	Analog to Digital Converter
AGC	Automatic Gain Control
BS	Beam Splitter
CMRR	Common Mode Rejection Ratio
DSP	Digital Signal Processor
IA	Implementation Agreement
LO	Local Oscillator

Glossary	Info.
MGC	Manual Gain Control
MPD	Monitor Photodiode
MSA	Multi-Source Agreement
OIF	Optical Internetworking Forum
PBS	Polarization Beam Splitter
PCB	Printed Circuit Board
DP-QPSK	Dual Polarization Quadrature Phase Shift Keying
DP-16QAM	Dual Polarization Quadrature Amplitude Modulation
OTU4	Optical Transport channel Uint-4
CD	Chromatic Dispersion
PDL	Polarization Dependent Loss
SOP	State of Polarization
DGD	Differential Group Delay
SOPMD	Second Order Polarization Mode Dispersion

17. Technical Figure 1



18. Revision History

Version	Date	Description	Prepared by
V6	2025	Unified WincoTek datasheet format	WincoTek
V6.1	2026-10-23	Engineering and format review	WincoTek